Special Issue!

IEEE Grid

AUGUST 1993

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PEBBLE BEACH CA 93953

idea'93 *Wescon/93*

The Santa Clara Valley (IEEE), Power Engineering Society and the
Power Electronics/Controls Laboratory, Department of Electrical Engineering, San Jose State University
present a professional course on

DYNAMIC ANALYSIS AND SPECIAL APPLICATIONS OF ADJUSTABLE SPEED DRIVES

co-sponsored by Electric Power Research Institute and Pacific Gas and Electric Company

Thursdays, September 9 - December 16, 1993
7:00 - 10:00 p.m.
San Jose State University College of Engineering, Room 301

THIS COURSE IS DIRECTED AT PRACTICING ENGINEERS involved in the application, maintenance and design of adjustable speed drive systems.

The course will concentrate on the dynamic operation of conventional and modern drive technology. Dynamic models of the dc motor, ac induction motor, wound field, and permanent magnet synchronous (brushless dc) motor will be developed in detail. These are nonlinear dynamic models and solutions will be provided by computer simulation using tools such as Matrixx and Spice derivative programs. Participants will be encouraged to recommend and use other familiar computer modeling tools where appropriate. These models will then be supplemented with appropriate converter and mechanical load models to provide a complete drive system simulation for use in evaluating and specifying ASD application performance.

The class will emphasize hands-on use of the SJSU Computational Lab Facility using Matrixx/System - Build and Spice simulation tools. These will be used throughout the course for simulating different drive systems. Additionally, the utility power system will be simulated to provide power quality data for different systems and the determination of compliance with the IEEE 519 power quality standard.

Advanced drive systems including the switched reluctance and switched reluctance/ Permanent Magnet hybrid machine will be covered. Two lectures by world class ASD experts will be provided to give the class an insight into the state of the art in ongoing drive development.

Who Should Attend

- consulting and plant engineers involved in specifying and maintaining drive systems
- modern control and computer peripheral engineers interested in drive technology beyond conventional DC drives
- utility engineers with an interest in adjustable speed drives and power quality
- matriculated electrical engineering students

Invited Guest Lecturers

Dr. Richard Hoft, Power Electronics Research Center, University of Missouri, Columbia
Dr. Thomas Jahns, Corporate Research and Development, General Electric Company, Schenectady, New York

Instructors

Dr. William L. Erdman, U.S. Windpower, Power Electronic Development
Dr. Ping Hsu, Department of Electrical Engineering, San Jose State University

FOR MORE INFORMATION OR AN SJSU CAMPUS MAP, PLEASE CALL (408) 924-2600 OR (408) 370-4000.
FOR PARKING INFORMATION, CALL (408) 924-6556.

Registration Form - Dynamic Analysis and Special Applications of Adjustable Speed Drives - EE 196R

Thursdays, September 9–December 16, 1993
7:00 - 10:00 p.m.
Fee: $595
The first 20 IEEE members to register will receive a $50 rebate.

Please register me for the IEEE co-sponsored Dynamic Analysis and Special Applications of Adjustable Speed Drives course.

Make check payable to: San Jose State University and mail registration form to: Continuing Education, San Jose State University, San Jose, CA 95192-0135, or call (408) 370-4000 or (408) 924-2600 to register with VISA or MasterCard. You may fax this form to (408) 370-4003.

Name_____

Social Security Number_____ IEEE Member Number_____

Organization/Company_____

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City_____ State _____ Zip _____

Daytime telephone (_____) _____

Amount Enclosed_____

☐ VISA ☐ MasterCard Account #_____

Signature_____

Do you wish to audit or receive a grade for this course? ☐ Audit ☐ Letter Grade

IEEE Grid

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Monthly Newsmagazine of the
San Francisco Bay Area Council of
The Institute of Electrical and Electronics Engineers, Inc.

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Bay Area Council
1992-1993

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Top of the News

Value Engineering and Total Quality Management Added to Wescon Short Course Program

A late entry into the Wescon Short Course Program has been announced. Course No. 15 will be "Value Engineering and Total Quality Management: A Joint Approach to Global Success," and will be taught by Kamal K. Mirchandani, PE, of GEZ Architects Engineers, San Francisco. The course will be offered Wednesday, September 29 from 10:00 a.m. to 12:00 Noon.

The course presents an overview of value engineering methodology which is fast expanding into the management culture of businesses covering products, services, manufacturing and construction industries. Together, value engineering and total quality management (TQM) are entering a global phase where the cost of material and labor are not the only concerns, but other factors such as time to market, cost of doing business and after sales service also merit equal consideration.

The course covers application of FAST diagrams leading to understanding of function analysis in a multi-discipline team environment. Combined with quality improvement, the function analysis technique helps enhance the overall value of the project in a cost-effective manner. Several examples of FAST diagrams and quality function will be presented.

The instructor, Kamal Mirchandani, is vice president of GEZ Architects Engineers, a firm that provides value engineering and facility design services to scientific and technology corporations, as well as to government agencies. Mirchandani is a professional electrical engineer, registered in six western states. He is a senior grade member of IEEE.

continued on page 34

IEEE Grid is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical & Electronics Engineers. As a medium for both news and opinion, the editorial objectives of The Grid are to inform its readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area.; to publish the official calendar of events; to report on IEEE activities on a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials, and letters to the editor.

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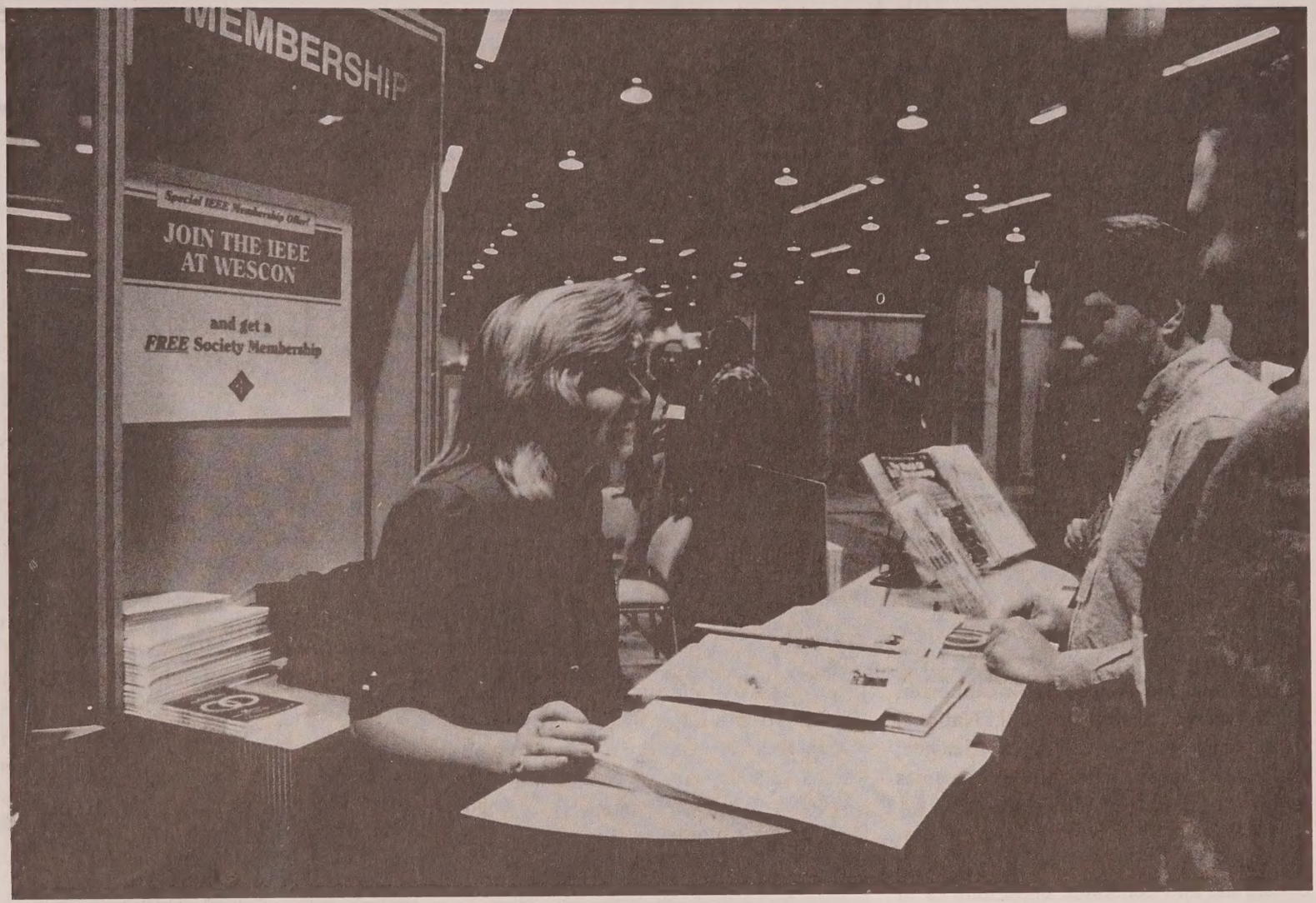


idea'93 and *Wescon/93*

The only exposition and conference specifically for the ASIC, programmable device and EDA industries joins America's largest OEM electronics conference and exhibition–together for the first time in one location!

Moscone Convention Center
San Francisco
September 28-30, 1993

More than 1,000 exhibits, two technical conferences and much, much more will be presented when Wescon/*idea* opens on September 28. We are pleased to bring you, in this special issue of the IEEE Grid, a preview of this spectacular event. On the following pages, you'll find detailed descriptions of both technical programs, plus all the special events being offered, and a product showcase, announcing some of the new technology being presented on the exhibit floor.

We have included special registration forms for all the events described, along with pricing information for the various elements of the conference. Please keep in mind the show is still more than a month away, and some information might be subject to change. More information and a preview program with complete show details are available by calling 1-800-877-2668.

Join Us At These Wescon/93 Special Events

Tuesday, September 28, 1993 Executive Day

The Wescon/93 Executive Day program is a rare opportunity for high-level managers to meet with industry experts to discuss business and economic issues facing the electronics industry in today's changing domestic and global marketplace.

Economic Forecast Explores Opportunities in the Pacific Rim

Many of our nation's top electronics equipment manufacturers utilize electronic components, parts and subsystems from Pacific Rim regions, including Taiwan, Hong Kong, China, and Korea. Apple Computer, Intel, AMD, Hewlett-Packard, National Semiconductor, Motorola, AT&T, Seagate, and Maxtor are just a few of the companies with facilities located in this area.

The Wescon/93 Economic Forecast provides a special look at international trade conditions and economic opportunities in the Pacific Rim. The program will feature two distinguished speakers: Peter Johnson, Director of the Hong Kong Economic and Trade Office in San Francisco, and Eden Chen, Ph.D., Principal Consultant, CTI. Each will share valuable information about Pacific Rim countries, and discuss how the electronics industry can benefit from their combined resources.

The Economic Forecast will be held Tuesday, September 28, 9:30 a.m. - 11:00 a.m., Room 220/222, Moscone Convention Center. Tickets are $25. Reserve your seat now. Register using the coupon on page 23.

Special Executive Day Program multi-event discounts available.

Keynote, Economic Forecast and Business Conference $70; Keynote and Economic Forecast $50; Keynote and Business Conference $50.

Cirrus Logic's Michael Hackworth to Deliver Keynote Address

Michael L. Hackworth, President and CEO of Cirrus Logic, Inc., will deliver the Wescon/93 keynote address, "Wireless Communication: The New Frontier," during a special luncheon on Tuesday, September 28.

Hackworth has over two decades of experience in the semiconductor and electronic components industries. Before joining Cirrus Logic in 1985, Hackworth spent fourteen years at Signetics Corporations (a subsidiary of N.V. Philips, the seventh largest semiconductor company worldwide), most recently as Senior Vice President. There he was responsible for staffing and directing that company's successful entry into MOS technology. He also guided a series of joint development programs with Motorola (for the 68000 processor family) and Intel (for the 8051 processor family).

Prior to his work at Signetics, Hackworth held a variety of marketing and sales management positions at Motorola and Fairchild Semiconductor.

The keynote luncheon will take place at noon in the Seacliff Room at the San Francisco Marriott. Tickets are $35. Reserve your seat using the form on page 23.

Business Conference to Discuss Economic Renewal in Silicon Valley

The Wescon/93 Business Conference will offer a unique opportunity to hear from leaders of Joint Venture: Silicon Valley, a revolutionary public-private sector movement dedicated to implementing a package of economic remedies to deal with the challenges facing the region. Launched in January 1992, JVSV is pursuing a two-phase program of economic renewal, encompassing diagnosis of the current economy, as well as a series of economic initiatives for implementation.

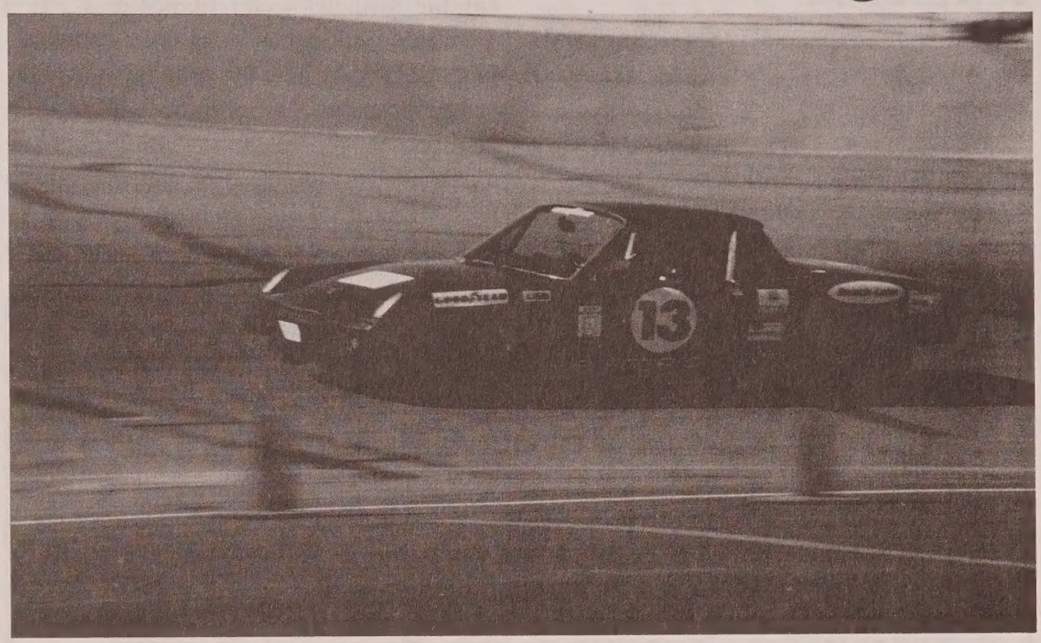
This informative panel will discuss the needs that prompted the group's formation, as well as its collaborative efforts to prepare Silicon Valley for the 21st Century. Panelists will also explore several JVSV initiatives, including Smart Valley and the Silicon Valley Global Trading Center.

Scheduled panelists include: Tom Hayes, Corporate Relations Manager, Applied Materials, Inc.; William Miller, Professor of Public and Private Management, Stanford University; Doug Henton, President, Collaborative Economics, Inc.; and James C. Morgan, Chairman and CEO, Applied Materials, Inc.

The Business Conference will be held Tuesday, September 28, from 2 p.m. - 4 p.m., Room 220/222, Moscone Convention Center. Tickets are $25.

Wescon Highlights Electric Vehicle Innovations With Showcase, Technical Session and Panel Programs

Co-sponsored by the Electrical Automobile Association



Electric Porsche 914 Targa on track during APS Solar and Electric 500 Race at Phoenix International Raceway, March 6 and 7, 1993. Stock A&B race. Driver: Ron Rasmussen of Santa Cruz. Photo by Paul Brasch.

The emergence of the electric vehicle industry has particular relevance for the nation's military/aerospace companies, as they seek new commercial markets in the face of reductions in defense spending.

The future of the electric vehicle industry depends heavily on battery technology. A special technical session, part of the Wescon Technical program, will explore several developments in battery technology, including an advancement in the thin film polymer battery, and improvements in the conventional lead acid battery. The session will also cover fast charging of electric vehicle batteries, as well as precision energy monitoring to measure battery energy.

A special electric vehicle panel program, co-sponsored by the Electric Automobile Association, has been scheduled for Thursday, September 30, 2 p.m. - 4 p.m. Composed of long term electric car users, the panel will explore the past and future of electric vehicles, with specific focus on motivation, technology costs, reliability, performance, safety, handling and support issues.

You'll also have an opportunity to see the latest electric vehicle innovations in a Featured Exhibit electric vehicle showcase, located on the exhibit floor. The showcase will feature commercially available vehicles, as well as race cars, utility company vehicles and Electric Automobile Association vehicles. Cars from companies and individuals such as Ford Motor Company, GM, Battery Automated Transportation, Inc., ElectroAutomotive, California Electric Cars, Dolphin Electric Vehicles, Doran Motors, Solar Electric Engineering, Clare Bell and Ron Rasmussen, Scott and Anna Cornell, Bob Schneevais, and the Solar & Electric Racing Association, are scheduled for display.

The showcase exhibit will be open each show day, 9 a.m. - 5 p.m., except Thursday, 9 a.m. - 4 p.m.

Wednesday, September 29, 1993

Purchasing Conference: "Gearing Up For Success with Cross-Functional Teams"

In today's competitive environment, the most effective companies are those that "team up for success" with a cross functional team model. By knocking down the walls that have divided functions in the past, key players can pool their skills, knowledge and experience to improve quality and efficiency, and achieve significant cost savings.

The Wescon/93 Purchasing Conference will explore the experiences of companies that have successfully used the Cross Functional Model, and discuss how your company can develop and benefit from cross functional teams. The conference will cover such topics as:

- What are Cross Functional Teams?
- Who should be involved?
- Team dynamics
- How they function

Don't miss this opportunity to learn from two distinguished purchasing professionals at Wescon/93.

Speakers: Peggy Williams is Director of Supplier Management for Sun Microsystems. She has extensive purchasing and inventory control experience in the aerospace and defense, medical, electronic, nuclear and computer industries. Williams is a past recipient of the Edwin G. Chambers Award and the Professional Development Person of the Year Award presented by the National Association of Purchasing Management.

Laurie Stover, materials manager at Lam Research Corp. in Fremont, Calif., has worked in the Materials profession since 1973. Prior to joining Lam Research Corp., Stover worked at several leading high tech companies, including Motorola, Advanced Micro Devices and Apple Computer. She has held various positions in the Materials field, including Materials Controller, Production Manager, Shipping/Receiving and Stores Manager, and Purchasing Manager. She is a member and past vice president of the Silicon Valley Chapter of the National Association of Purchasing Management.

The Purchasing Conference will be held Wednesday, September 29, 9:30 a.m. - 11:30 a.m. in Room 220/222, Moscone Convention Center. Tickets are $25. Plan now to attend. Register using the coupon on page 00

Special Session Explores "Issues in OEM Systems Integration"

As part of its expanded focus on the OEM/ Computer Systems and Subsystems market, Wescon will present a special tutorial session addressing "Issues in OEM/Systems Integration."

Sponsored by Computer Design magazine, the session will cover topics in concurrent engineering, design-for-test, design-for-manufacturing, total quality management, marketing considerations in product design and development, and overcoming obstacles to communications. Panel members will represent major vendors of ICs, tools or system components, consultants in concurrent engineering or total quality management, as well as product line managers from major OEM systems companies. The tutorial will be moderated by Mike Donlin, Senior Editor for CAE/CAD tools at *Computer Design* and Editor of *OEM Integration*.

The session will be held Wednesday, September 29, 2 p.m. - 4:30 p.m., Room 220/ 222, Moscone Convention Center. Plan now to attend. There is no additional charge for registered visitors to attend the special session.

CURTISPMC

A Division of Curtis Instruments, Inc.

CurtisPMC, in business for over 30 years, is a world leader in the design and manufacture of transistorized and microcontroller-based speed controllers, including applications for the industrial, recreational and invalid vehicle markets. We are a small global company and have strong customer demand to originate an advanced line of products for the electrical vehicle market.

Applications Engineer

Provide technical, application support to customers. Recommend new applications, customers, markets. Travel to customer sites for technical follow-up and sales support. Develop all technical documentation as required. BSEE or equivalent including courses in analog and digital design, and control system design. 5+ years experience required. Sufficient experience to understand usage and design of electronic components. Ability to go from concept of operation to design of a circuit executing the operation.

Software Engineer (2)

This is a mid-level design position developing real time embedded software and digital electronics for microcontroller-based products. Requirements include BSCS/BSEE or equivalent plus 4 years applicable design experience in product development environment. Strong assembly language; C also desired.

Senior Mechanical Engineer

Lead mechanical design projects. Conceptualize, design, analyze, fabricate, test, and assemble various mechanical and electromechanical assemblies, test fixtures and product packaging. BSME or equivalent. Project leadership skills, and an ability to independently conceptualize, develop and execute approaches (both "ballpark" and detailed) in a product development environment. Must be comfortable with electronics and capable with electromechanical assemblies. Experience with stampings, extrusions, injection moldings, castings, electronic packaging. Shop experience—mill, lathe, other power tools desired. Aesthetic sense and "production aware." Mechanical package design, thermal design, CAD experience.

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Curtis PMC, 6591 Sierra Lane, Dublin, CA 94568. FAX: 510-833-8777

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EQUAL OPPORTUNITY EMPLOYER

VXIbus Consortium Seminar and Hands-on Workshops Explore the Impact of VXI Technology

The VXIbus is a growing platform for instrumentation systems. First introduced in 1987, the VXIbus has experienced tremendous growth and acceptance around the world. Today, over 250 companies support VXI, and more than 600 products are available. Market studies estimate that by the year 2000, roughly half of all the instrument and measurement systems will use VXI.

Learn how VXI technology will affect your future at a special seminar and hands-on workshops led by the VXIbus Consortium and sponsored by the Santa Clara Valley chapter of the Instrumentation & Measurement Society. The full-day seminar will present in-depth information on the VXIbus specification, including device types and communication protocols. VXI system configurations, including the different methods for controlling and programming a VXIbus system, will also be discussed. The seminar will be held at Moscone Convention Center, Tuesday, September 28, 9 a.m. - 5 p.m. Workshops will take place in one-and-a-half-hour increments each day throughout Wescon.

Wescon/idea Product Showcase begins on page 24

Travel to *idea* and Wescon:

PARKING

Cow Palace: Park at the Cow Palace in Daly City and ride the FREE *idea /Wescon* SHUTTLE to Moscone Convention Center. *idea '93* show directories will be available at the Cow Palace. Let our drivers deal with the traffic, while you relax and plan your day at *idea* and Wescon. Lots of parking available at $5 per car.

Downtown: A discounted rate of $7 per day is available to *idea/Wescon* attendees at the Moscone Center Garage, located at 255 3rd Street. There are several other parking lots within walking distance to the Moscone Convention Center. Detailed information will be provided in the *idea/Wescon* Transportation Brochure, which will be mailed with your registration badge.

Colma: Free parking is available at D Street and Junipero Serra (off Hwy. 280). Complimentary Samtrans bus service every 5 minutes during commuter hours (6:15am - 9:20am and 3:25pm - 6:20pm, Monday through Friday) is available to the Daly City BART Station.

BART/MUNI

The BART/MUNI METRO Powell Station at 4th and Market is closest to the Moscone Convention Cetner. If you're riding the Muni, take the 45 Union or 30 Stockton for Moscone Center. For BART schedule and rate information call (415)464-6000. Detailed BART information will be provided in the Transportation Brochure which will be mailed with your registration badge.

CAL-TRAIN: THE *idea/Wescon* EXPRESS

Use Cal-Train as your *idea/Wescon* Express. Take the train from Silicon Valley to the Southern Pacific Depot in San Francisco. Continuious complimentary *idea/Wescon* shuttle service from the depot to Moscone Center is provided. *idea/Wescon* show directories and plenty of parking will be available at the Sunnyvale Cal-Train station. Call (800)660-4287 (Bay Area) or (415)508-6200 (outside the Bay Area) for Cal-Train schedule information.

Complete transportation and parking information will be included with your registration badge. For telephone assistance, call (800)877-2668 or (310) 215-3976, ext. 219, 235 or 242.

Where to Find it!

All *idea '93* and Wescon/93 exhibits, technical conferences and special events, except the Wescon keynote luncheon, will be held at Moscone Convention Center at 747 Howard Street in San Francisco. The keynote luncheon will be held at the San Francisco Marriott, 777 Market Street, two blocks from the convention center.

Conference and exhibit hours are Monday, September 27 (*idea* training courses only) - 9:00 a.m. to 5:00 p.m.; Tuesday, September 28 - 9:00 a.m. to 5:00 p.m.; Wednesday, September 29 - 9:00 a.m. to 5:00 p.m.; Thursday, September 30 - 9:00 a.m. to 4:00 p.m.

The registration area will be located at the North and South lobbies of the convention center.

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We've got the work. Can you meet the challenge?

TRW's Electronic Technology Division has been designing and producing leading edge communication and processing systems for the nation's most critical space programs for over 35 years. Newly funded projects, and increased funding for ongoing programs, have created multiple opportunities for experienced engineers with proven capabilities in the application of advanced technologies:

Communication System Engineers
Analysis, simulation, design and delivery of space borne payload and ground-based communication systems. Requires experience in RF, digital, baseband communication & signal processing systems; networks; modulation/demodulation; and detection & estimation. MSEE or PhDEE, 3-5 years experience.
Steve Lunny, R6/1432, fax (310) 813-4719.

Digital ASIC Design Engineers
All aspects of ASIC design and development, MENTOR/SYNOPSYS experience strongly desired. BSEE/MSEE, 3-5 years experience.
Ron Smith, M5/2132, fax (310) 814-3199

Digital Signal Processing/Communication System Hardware Designers
Digital demodulators, digital modulation techniques, and SPW/BOSS tool experience preferred. BSEE/MSEE with 3-10 years experience.
Ron Smith, M5/2132, fax (310) 814-3199.

Sr. Analog IC Design Engineer
Custom analog IC design and analysis of silicon bipolar and GaAs technology circuits, architectural trade-offs, design, and layout. BSEE, 2 years custom IC design, and familiarity with MENTOR/CADENCE and A/D converters.
Steve Mishima, M5/2565, fax (310) 814-3199.

Custom CMOS IC Design Engineers
VLSI projects. Responsibilities include logic design, layout, and verification. Familiarity with MENTOR GDT and COMPOSE desired. BSEE/MSEE.
T. Yu, M5/2476, fax (310) 814-3199.

Space Borne Processor Unit Design Engineers
Design and analysis for 16-bit and 32-bit fault tolerant processor units. Experience with 1750A and/or R3000 desirable.
D. Terry, M5/2067, fax (310) 814-3199.

HEMT and HBT Development Engineers
GaAs-based or InP-based HEMT or HBT MMIC wafer fab, RF circuit evaluation, and device physics. Requires proven record of innovation & originality in the IR&D of new processes & product development. Circuit design a plus. PhD in EE/Physics or related discipline, or MS degree with 5 years experience.
Ed Rezek, D1/1050K, fax (310) 814-4448.

HEMT and HBT MMIC Product Engineers
Insertion applications for HEMT or HBT MMICs. Must interface with MIMC product designers. Knowledge of related MIL Standards, SPC and TQM a plus. PhD in EE/Physics or related discipline, or MS degree with 5 years experience.
Ed Rezek, D1/1050K, fax (310) 814-4448.

Product Engineers
Electronic packaging of spacecraft and commercial RF and digital hardware. Teamwork, communication/interpersonal skills a must. CAD experience highly desirable. BSME required.
Michael Stull, R6/1194, fax (310) 813-5141.

Stress and Thermal Analysts
Structural and thermal analyses on electronic and electro-mechanical equipment. Strong analytical and modeling skills, good communication skills, and proficiency with NASTRAN or SINDA a must. BS/MS degree and 5 years experience.
Wes Sakamoto, R6/1176, fax (310) 814-5141.

We offer an excellent benefits package, highly competitive salaries, and some of the most interesting high-tech positions available. For immediate consideration, please mail/fax your resume to the contacts listed above at: **TRW, One Space Park, Redondo Beach, CA 90278.**
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BESSER ASSOCIATES

offers three courses on

RF/HIGH-SPEED ANALOG CIRCUIT DESIGN

These short courses were developed for engineers, technicians and managers who design, produce, and test RF/MW circuits and systems. The courses also help high speed digital engineers understand analog techniques. Interactive video projection of CAE tools is included in lectures.
The courses are held at Golden Gate University, Los Altos CA

I. RF Fundamentals and Passive Circuits

August 25-27, 1993

Instructor: Les Besser

DAY 1 - Scattering parameters and the Smith Chart
DAY 2 - Networks and modeling
DAY 3 - Transmission lines and CAE Techniques

Switching from traditional definitions based on voltages and currents, to power-flow concepts and scattering parameters, the course smoothly transitions into the high frequency domain. First, we become familiar with a relatively simple, yet powerful graphical design tool--the Smith Chart--that is used throughout the course. We also examine component models in their physical forms, discussing parasitic effects and losses, revealing reasons why inductors and capacitors often behave in surprising manners at RF. Filters, resonant circuits and their applications are reviewed through filter tables and modern CAE techniques, leading into matching networks and matching filter structures. Since wires and printed circuit conductors may behave as transmission line elements, we include a session on microstrip, coaxial and twisted wire transmission line realizations. The course concludes with a discussion on PIN diode switches and attenuators.
Two CAD programs, PUFF and EEZMatch are given to all participants.

II. Linear and Large-signal Amplifiers

August 30- September, 1 1993

Instructors: Les Besser, Steve Cripps

DAY 1 - Linear Amplifiers
DAY 2 - Nonlinear Circuits I
DAY 3 - Nonlinear Circuits II

Narrow- and broad-band small-signal amplifier designs are introduced via s-parameter techniques, considering both unilateral and bilateral techniques. Negative feedback applications, using lossy and lossless feedback networks are introduced and illustrated via broadband amplifier design examples. Stability and layout effects are also discussed. Large-signal amplifiers are first introduced by linear approximations, progressing to full nonlinear characterization. Special considerations are given to maximum power output, linearity, distortion, biasing and large-signal RF stability. Illustrative design examples are shown using real-life examples through interactive video presentation.

III. RF Receivers: Oscillators, Mixers and Low-noise Amplifiers

September 2-3, 1993

Instructor: Edward Niehenke

DAY 1 - Low-noise Oscillators
DAY 2 - Mixers and Low-noise Amplifiers

This course covers RF/MW oscillators, using both two-terminal and three-terminal devices. Topology selection, device interaction, and relationships considering phase-noise, output power, post-tuning drift, tuning speed, linearity, and stability are presented with examples of high-technology designs. Mixers and their applications are viewed from the integrated receiver's viewpoint. The latest low-noise design techniques using state-of-the-art FET and bipolar devices are also presented. Device equivalent circuits and noise models are related to matching network design. Amplifier stability, gain and noise trade-offs, and the effect of biasing are included.

Prerequisite:
BS(EE) graduates, or electronic technicians with at least three years practical experience

For registration and information call
BESSER ASSOCIATES
415/949-3300 FAX 415/949-4400

IEEE Region 6 Student Paper Competition

The 1993 IEEE Student Paper competition will be held Wednesday, September 29 from 1:00 PM to 4:00 p.m. In this session, the winners of each of the area student paper contests in IEEE Region 6 will present their winning papers. These will be judged and prizes awarded to the top papers.

Organizer/Chairman for this event is Dr. Bruce Johnson of the University of Nevada, Reno.

Paper No. 1
Video Thermometer and Humidity Indication
Michael Landrum
California State University, Los Angeles
Glendora, Calif.

Paper No. 2
Analysis of the Dielectric Slab Waveguide
Kate Remley
Oregon State University
Corvallis, Ore.

Paper No. 3
Transmission of Electronically Generated FSK Using a 1.3 æm InGaAsP Fabry-Perot Laser Diode
Timothy L. Jackson
California State University, Sacramento
Orangevale, Calif.

Paper No. 4
Interstitial Antennas for Arterial Plaque Ablation
Mark Orme
Corey Catten
University of Utah
Salt Lake City, Utah

Bay Area Engineer

IEEE News begins on page 27

Integrating Technology for System Design

The *idea'93* conference and exhibition will provide you with the information you need for successful system design in today's competitive, increasingly complex marketplace.

A comprehensive program of 36 seminars, 13 training courses, stimulating panel discussions and debates will address critical business and technical issues facing the ASIC, FPGA and EDA industries. Presented from a users perspective, this applications-oriented forum will provide you with practical knowledge you can use today to improve your productivity and effectiveness.

And on the exhibition floor, you'll be able to test drive the latest products from over 100 of the leading suppliers in the ASIC, FPGA and EDA markets. Companies such as Microsoft, Microsim, Mitsubishi, OrCAD, Protel, Racal-Redac, S-MOS and Viewlogic. This is an invaluable opportunity to gain hands-on experience with these products before you make crucial purchasing decisions.

Just one admission ticket provides access to both the idea and Wescon exhibitions.

Attendees with specific and multiple product interests will find design solutions from leading suppliers of ASICs, programmable devices and EDA tools and software, as well as products from manufacturers of the latest in computer OEM systems and subsystems, test and measurement instrumentation, and production materials and services.

Three-day conference seminar registration includes unlimited attendance to all *idea* seminars, *idea* exhibits, Wescon exhibits, Wescon technical sessions, as well as a copy of the *idea* Conference Proceedings. Registration is $250 by 9/3/93, $350 after 9/3/93.

One-day conference seminar registration includes unlimited attendance to all *idea* seminars on that particular day, *idea* exhibits, Wescon exhibits, and Wescon technical sessions.

Registration is $100 by 9/3/93, $150 after 9/3/93.

Training registration includes instruction materials, admission to *idea* and Wescon exhibits and the Wescon Technical Sessions. Training registration does not include a copy of the *idea* Conference Proceedings. Registration is $175 (half-day) by 9/3/93, $225 after 9/3/93. Registration is $295 full-day (2 half-days) by 9/3/93, $395 after 9/3/93.

Half-day training registration and 3-day seminar registration includes instruction materials, admission to *idea* and Wescon exhibits and the Wescon Technical Sessions, as well as a copy of the *idea* Conference Proceedings. A copy of the Wescon Conference Proceedings is not included. Registration is $375 by 9/3/93, $475 after 9/3/93.

Full-day training registration and 3-day seminar registration includes instruction materials, admission to *idea* and Wescon exhibits and the Wescon Technical Sessions, as well as a copy of the *idea* Conference Proceedings. A copy of the Wescon Conference Proceedings is not included. Registration is $495 by 9/3/93, $595 after 9/3/93.

The idea Technical Conference was organized by industry experts from leading companies in the ASIC, FPGA and EDA industries. *idea* gratefully acknowledges their support: **Tom Anderson,** Kubota Pacific; **Yatin Trivedi,** YT Associates; **Jean-Pierre Braun,** Sunrise Test Systems; **Keith Dow,** Vertex; **Dennis Leitterman,** Hewlett-Packard; **John Prince,** Intergraph Electronics; **Mahendra Jain,** Compass Design Automation; **Jesse Jenkins,** ASIC/FPGA Consultant; **Tom Wong,** Hitachi America Ltd.; **Charles Weaver,** Delfin Systems; and **Chris Malachowsky,** NVidia Corp.

Seminar and training attendees automatically receive free admission to the *idea* exposition. For those who wish to visit the exposition only, complimentary registration is available using the coupon on page 23 or by calling 800-877-2668.

idea Training Courses Monday, September 27

9:00 a.m. to 12:30 p.m.

T1 Introduction to ASICs *C. Malachowsky*	**T2** Introduction to Verilog HDL *Y. Trivedi*	**T3** The Critical First Lesson in VHDL *I. Finlay, J. Pick*	**T4** High-Speed Interconnect Modeling with SPICE *K. Dow, E. Bogatin, C. Wyland*	**T5** Design for Testability *T. Niermann, S. Chandra*	**T6** Formal Methods for Digital Hardware Design *P. Lowenstein*	**T7** Introduction to MCMs *P. Franzon*	**T8** Designing High-Speed Products that Work *J. Blankenhorn*

1:30 p.m. to 5:00 p.m.

T9 Maximizing Quality in the Electronic Design Cycle *S. Sapiro*	**T10** Designing for FPGAs *R. Awalt*	**T11** Circuit Simulation Using SPICE 3 *J. Hines*	**T12** Systematic ASIC Development *C. Shelor*	**T5** Design for Testability *T. Niermann, S. Chandra*	**T13** High Performance Packaging *P. Franzon, K. Dow, C. Wyland*		

Panel Discussions

Expert panelists will debate the pros and cons of the hottest topics in ASICs, FPGAs and EDA each day at *idea'93*.

Tuesday, September 28, 1993
Panel #1
1:00-2:30 PM
Life in the Synthesis Jungle
Moderator: John Cooley, EDA and ASIC Design Consultant
Panelists: Moshe Kohen, i-Logix
Ewald Detjen, Exemplar Logic
Tom Anderson, Kubota Pacific
Adel Khouja, Synopsys
Ken McElvain, Mentor Graphics
Homayoun Mavahed-Ezazi, Cadence

Wednesday, September 29, 1993
Panel #2
12:00-1:30 PM
Protecting Intellectual Property in the EDA Industry
Description: This panel gives an overview of the issues involved with intellectual property protection, especially for software. Panelists are representatives from the legal community, EDA company executives and others who provide unique and valuable perspectives and experience.
Moderator: Ronald Collett, Collett International Inc.
Organizer: Dr. William vanCleemput, Delos Research Group
Panelists: Philip P. Berelson, Brown and Bain
Ewald Detjens, Exemplar Logic
Dr. Bernard Galler, Industrial Technology Institute
Dennis Fernandez, Fenwick and West
Susan Nycum, Baker and McKenzie
Richard M. Stallman, League of Programming Freedom

Thursday, September 30, 1993
Panel #3
12:00-1:30 p.m.
Mining the Federal Labs
Description: Dramatic changes in the United States budget structure are causing dramatic changes in the way that the national labs are doing business. This panel session features representatives from a number of government entities who will explain the changing role of the national labs and how American businesses can tap into the wealth of talent and resources that were previously off limits to the general public.
Moderator: Grant Stockdale

Training

Monday, September 27, 1993
PRACTICAL SOLUTIONS FOR SYSTEM SUCCESS - All training programs will be held Monday September 27, 1993. Training programs are intensive half-and full-day courses conducted by acknowledged industry experts and designed to give you "how-to" understanding of ASIC, FPGA, and EDA business and technical issues. You'll gain substantial, practical information and instruction that you can implement immediately to solve your system design issues.
Pricing:
(half-day) $175 by 9/3/93- $225 after 9/3/93
Full-day (2 half-days) $295 by 9/3/93 - $395 after 9/3/93
Pre-registration is encouraged. Courses are subject to cancellation two weeks prior to show (September 13, 1993) if minimum number of registrants is not met. Registration at the door will be accepted on a first-come, first-serve basis with no guarantee of space or class materials. NO REFUNDS WILL BE MADE AFTER SEPTEMBER 23, 1993. Company discounts for some courses are available upon request.
9 a.m. - 12:30 p.m.
T1
Introduction to ASICs
What does a designer need to know to succeed with an ASIC design? What tools are needed? What skills are required? This training course will answer these questions and survey the gamut of technologies, methodologies, and topics relevant to anyone trying to deliver an ASIC-based design solution. Emphasis will be on-digital CMOS gate-array and standard cell designs. The training course will cover both logical (front end) and physical (back end) design processes.
Instructor: Chris Malachowsky is a founder and VP of engineering of NVidia Corp., a firm specializing in graphic accelerator design. For 10 of his 13 years of industry experience, he has been involved in designing, verifying, and shipping some of the computer industry's largest and most complex ASICs. Starting with a 20K gate standard cell CPU in 1985, when he worked for Hewlett-Packard, up to multiple 100K+ gate graphic accelerator (gate array, standard cell, and structured custom) chips for Sun Microsystems, Malachowsky has learned by doing. He holds over 20 patents, has BSEE/MSCS degrees, and teaches a 10-week introductory ASIC course for UC Berkeley's graduate extension program.
9 a.m. - 12:30 p.m.
T2
Introduction to Verilog HDL
Hardware description languages (HDLs) have helped manage the increased complexity of devices (ASICs) and systems by providing multi-level abstraction, modeling, and verification capability to design engineers. Verilog HDL has been successfully used by several system and semiconductor manufacturers for modeling and verification of their designs. This training course presents an overview of the language–lexical components, data types, operators, expressions, and statements. Several short examples will be used to demonstrate the correspondence between the hardware and its model. Behavioral as well as structural models will be discussed. Some of the advanced topics, including user defined primitives, concurrent behavioral modeling, tasks, and timing analysis will be presented. Test vector generation and verification strategies will also be introduced. This training course is intended for design engineers involved in ASIC or board design who are considering the use of HDLs. Familiarity with a programming language and some design experience will be helpful. Those familiar with other HDLs may find this training course interesting for comparison purposes.
Instructor: Yatin Trivedi is well respected in the industry for his work with Verilog HDL. He co-authored the first book on Verilog, *Digital Design and Synthesis with Verilog HDL*. He is the editor of the Verilog HDL language Reference Manual (LRM) 2.0, published by Open Verilog International. He also writes a monthly column, "Inside HDL" for *ASIC & EDA* Magazine.
9 a.m. - 12:30 p.m.
T3
The Critical First Lesson in VHDL
The IEEE-1076 standard hardware description language, VHDL, is rapidly becoming a prominent component of the design, documentation, and simulation environment of the electronics industry. Consequently, it is very important for electronic engineers to rapidly understand the key design capabilities of this new CAD tool and environment. This training course will present an innovative approach for introducing the VHDL language. The big picture is presented via a series of examples that illustrate how the individual constructs actually fit together and interact. Additionally, caveats based on real-world design experiences are discussed and creative solutions to potential problems are illustrated in detail.
Instructor: Dr. Iain Finlay is currently working in the Synthesis Group of Compass Design automation, where he is a member of the VHDL Behavioral Synthesis System development team. In addition, he is part of the VHDL Training team at compass. His interests lie in the application of VHDL to High-Level (Behavioral)

Complimentary Exhibit Pass

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synthesis. Dr. Finlay received a Ph.D. from the Department of Electrical Engineering at the University of Edinburgh for research in High-Level (behavioral) Synthesis. He has an B.Sc. (Hons), First Class, in Electronics and Electrical Engineering.

9 a.m. - 12:30 p.m.

T4

High-Speed Interconnect Modeling with SPICE

This training course details how to convert a physical layout of interconnects on an MCM, package, or board into a SPICE netlist. The accuracy and limitations of the resulting netlist are covered in the training course as are techniques for experimental verification of the netlist

Instructors: Keith Dow has a B.S., M.S., and Ph.D. in physics. Previous experience includes three years managing a modeling group which was responsible for the generation of Spice CMOS and bipolar transistors models. He holds one patent for a high speed, low crosstalk digital interconnect. At the present time he is a senior multichip module engineer at Vertex Semiconductor with responsibility for high speed digital interconnect modeling.

Eric Bogatin has a B.S., M.S., and Ph.D. in physics. Thirteen years of experience in the industry include working for AT &T Bell Laboratories, Raychem and Bogatin Enterprises. He is the author of several articles and books on the field of interconnect modeling. At present he is a manager at Sun Microsystems in charge of "Process modules and new technologies."

Chris Wyland. has a BSME from the University of California, Santa Barbara. He has spent 3 years doing high performance package modeling and is currently working for Applied MicroCircuits Corporation doing high speed electrical package modeling. He has two patents pending for package designs and authored the paper "Comparison of Commercial Thermally Enhanced Quad Flatpack," ITHERM 1992. He has been a member of JEDEC JC-15 since its beginning.

9 a.m. - 5 p.m.

T5

Design for Testability

This training course is intended for ASIC designers, developers, and managers who want a broad overview of the state-of-the-art in strategies for testing of complex ASIC chips. CAD tool designers and managers will also find it useful to learn about the CAD tools in the area of testing. Contents include design for testability, automatic test pattern generation, fault simulation, level sensitive scan design, partial scan, the IEEE boundary scan standard, signature analysis, and built in self test (BIST). The only background required of attendees is some knowledge of logic design and a general familiarity with the ASIC industry.

Instructors: Thomas M. Niermann is a vice president of research and development at Sunrise Test Systems, Sunnyvale, California. He co-founded Sunrise Test in 1990. Dr. Niermann oversees the research and development of tools related to automatic test generation, fault simulation and synthesis for testability. He received his B.S. and M.S. degrees in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign. He is a member of the IEEE and the ACM.

Susheel J. Chandra is a senior CAD engineer with Sony Microsystems, where he is responsible for incorporating testability into their next generation of workstations. Dr. Chandra was previously with CrossCheck Technology, Inc. where he was responsible for the development of tools related to test generation, fault simulation, and testability. He received his M.S. and Ph.D. degrees in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign. He is a member of the IEEE.

9 a.m. - 12:30 p.m.

T6

Formal Methods for Digital Hardware Design

Increasing complexity of digital systems makes subtle design errors and misunderstandings both more likely to occur and more difficult to find. Formal methods are well adapted to avoiding these problems, finding errors, and resolving misunderstandings. The training course will cover the principal approaches to successfully apply formal methods in hardware design. The emphasis will be on breadth at the expense of depth to allow an informed choice of what to pursue further for your particular designs. No prior knowledge of formal methods will be expected.

Instructor: Paul Loewenstein studied engineering and electrical sciences at the University of Cambridge, England, and received a BA in 1971 and an MA in 1975. He started his career as a research engineer at Schlumberger, UK, then moved to Schlumberger, France, followed by Fairchild Semiconductor Research Center in Palo Alto, California. After leading a team designing a DSP chip, he started working on formal methods for digital chip design in 1987. His work progressed through the acquisition of Fairchild by National Semiconductor, and he spent 19 months at Stanford as an industrial visitor for National Semiconductor. Lowenstein joined Mitsubishi as manager for formal verification in 1990, then joined Sun Microsystems in 1991, and applied formal techniques mainly to the design and debugging of multiprocessor systems. Has published several papers on the application of theorem proving techniques to the design of sequential and concurrent systems.

9 a.m. - 12:30 p.m.

T7

Introduction to MCMs

This training course covers the information the engineer coming from a chip or board design background needs to know in order to design a multichip module. Areas of emphasis include technology, testability, and software design tools.

Instructor: Paul Franzon is currently an Assistant Professor in the Department of Electrical and Computer Engineering at North Carolina State University. He has over eight years experience in electronic systems design and design methodology research and development. During that time, in addition to his current position, he has worked at AT&T Bell Laboratories in Holmdel, NJ, at the Australian Defense Science and Technology Organization, as a founding member of a successful Australian technology start-up company, and as a consultant to the industry, including positions on Technical Advisory Boards. Dr. Franzon's current research interest includes design sciences/methodology for high speed packaging and interconnections systems and for high speed and low power chip design. In the past, he has worked on problems and projects in wafer scale integration, IC yield modeling, VLSI chip design and communications systems design. He has published over 45 articles and reports. His teaching interests focus on microelectronic systems building including package and interconnection design, circuit design, processor design and the gaining of hands-on systems experience for students. Dr. Franzon is a member of the IEEE, ACM and ISHM. He serves as the Chairman of the Education Committee for the National IEEE-CHMT Society. Dr. Franzon received a B.S. in Physics and Mathematics, a BE with First Class Honors in Electrical Engineering and a Ph.D. in electrical engineering from the University of Adelaide, Adelaide, Australia.

9 a.m. - 12:30 p.m.

T8

Designing High-Speed Products that Work

The issues involved in properly designing circuits using high-speed TTL, CMOS, or analog circuits operating above 30MHz are difficult to master. This training course presents the issues involved in designing high-speed circuits. Included is information on controlled impedance

structures, non-controlled signal lines, termination, impedance, coupling, design guidelines, and more. It is an essential course for anyone involved in high-speed products.

Instructor: James Blankenhorn has been an engineer in electronics for twenty years and has been instructing while managing design departments in SMT since 1983. He established the first design guidelines published in the United States, many of which are used in the IPC guidelines. He has written over twelve books on SMT, taught numerous training courses, lectured at universities, and has been speaker and course chairman for many conferences. He holds a BSEE from Arizona State University.

1:30 p.m. - 5 p.m.

T9

Maximizing Quality in the Electronic Design Cycle

This training course is for engineers and managers who want to know how to get their product to market on time and with high quality. The training course includes techniques and case studies. Topics covered include how to get high quality, fault modeling, test development tools, and improving the testability of your design.

Instructor: Steve Sapiro has an extensive background in hardware and software design and was a founder of CAE Systems, Inc. and proCASE Corp. He has been an independent consultant for over six years for both CAE vendors and electronics system design users. He has published over twenty articles and two books.

1:30 p.m. - 5 p.m.

T10

Designing for FPGAs

Field programmable gate arrays offer a broad range of design possibilities. This training course explores the real-world tradeoffs among various FPGA architectures and tools. It examines which architectures are appropriate for various applications, and looks at the kind of performance that you can expect to achieve. This training course is a must for anyone beginning to use FPGAs.

Instructor: Rocky Awalt has nearly 30 years electronics industry experience. He attended Cleveland Institute of Electronics and San Jose State University. He has been with such companies as Lockheed, Four Phase Systems and Echo Communications, and was founder and president of Molecular Computer. Since 1988 he has been designing with FPGAs, and he is a principal and CEO of HighGate Design, digital design consultants, specializing in the use of FPGAs.

1:30 p.m. - 5 p.m.

T11

Circuit Simulation Using SPICE 3

This introduction to circuit simulation demonstrates how SPICE eliminates or reduces the need for breadboard testing of analog circuit designs. The training course uses fifteen common circuit design problems to show how SPICE will find and solve common problems before prototypes are available for testing. Three of the problems require new simulation techniques only available in SPICE 3, demonstrating why SPICE 3 is a "better SPICE."

Instructor: John R. Hines, RPE, is a silicon sensor engineer for MICRO SWITCH. He holds four patents on circuit design and two patents on the design of silicon sensors. He is a columnist for *IEEE Spectrum* and has written columns for *Design Automation* and *Electronics Test*. He has also written four books on circuit simulation which are distributed by Oholiab Technology (Richardson, Texas).

1:30 p.m. - 5 p.m.

T12

Systematic ASIC Development

The Systematic ASIC Development training course will discuss the application of an object-oriented process using VHDL based logic synthesis to the development of FPGAs and custom mask ASICs. Technical issues will include partitioning guidelines, use and limitations of VHDL based logic synthesis, testability, and system verification. Program issues will include cost and schedule estimating, tracking progress, peer reviews, concurrent engineering, and documentation requirements.

Instructor: Charles Shelor has 16 years experience in design and management of embedded computer systems using advanced microprocessors. He has extensive experience with computer-aided engineering tools and techniques including VHDL and logic synthesis. He received his BSEE and MSEE from Louisiana Tech.

1:30 p.m. - 5 p.m.

T13

High-Performance Packaging

The successful design of a high-performance package requires expertise in electrical, microwave, and mechanical engineering. What you need to know from these three fields is presented in detail along with mistakes to avoid.

Instructors: Paul Franzon is currently an Assistant Professor in the Department of Electrical and Computer Engineering at North Carolina State University. He has over eight years experience in electronic systems design and design methodology research and development. During that time, in addition to his current position, he has worked at AT&T Bell Laboratories in Holmdel, NJ, at the Australian Defense Science and Technology Organization, as a founding member of a successful Australian technology start-up company, and as a consultant to the industry, including positions on Technical Advisory Boards. Dr. Franzon's current research interest includes design sciences/methodology for high speed packaging and interconnections systems and also for high speed and low power chip design. In the past, he has worked on problems and projects in wafer scale integration, IC yield modeling, VLSI chip design and communications systems design. He has published over 45 articles and reports. His teaching interests focus on microelectronic systems building, including package and interconnection design, circuit design, processor design and the gaining of hands-on systems experience for students. Dr. Franzon is a member of the IEEE, ACM and ISHM. He serves as the Chairman of the Education Committee for the National IEEE-CHMT Society. Dr. Franzon received a B.S. in Physics and Mathematics, a BE with First Class Honors in Electrical Engineering and a Ph.D. in electrical engineering from the University of Adelaide, Adelaide, Australia.

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Seminars

LEARN FROM THE EXPERTS - Led by experienced users specifically chosen for their proven expertise, seminars are 60-minute presentations that address technical and business issues in the following areas: design automation, application specific ICs, programmable logic, and system development. You'll come away with a solid understanding of your most important issues and how to solve them with today's newest and best technologies.

Pricing: (3 days) $250 by 9/3/93 - $350 after 9/3/93; (1 day) $100 by 9/3/93 - $150 after 9/3/93

Tuesday, September 28, 1993

S1
9 a.m. - 10 a.m.
Notebook Computer Power Management Strategies Employing PLDs
Robert Bielby, Altera Corp.
Notebook computers are measured by several criteria: performance, size, weight, and power consumption. As advances in microprocessor and component technologies have led to more powerful, compact systems, power consumption is most recently gaining greater industry interest. This seminar reviews several different power management strategies employed in notebook computers and how they can be addressed using versatile, 3.3 volt, 12 ns programmable logic devices.

S2
10:30 a.m. - 11:30 a.m.
Demystifying Programmable Logic with Metric Benchmarks
Jay Sturges, Intel Corp.
The primary objective of the tutorial is to introduce a new way people can learn about programmable logic architectures. This is to say; the method(s) used in choosing the best suited programmable logic device, PLD, (whether PAL, PLA, CPLD, or FPGA, etc.) for the embodiment of a circuit subsystem. I believe that the practice(s) now have the opportunity to change from one that could only be performed through rules-of-thumb and historical information, to one that can be studied with real measurements. The tutorial presents the approach to demystify the correlation between what a circuit subsystem needs and how the subsystem matches up to what a specific PLD offers - It emphasizes a quantitative approach to the architectural trade-off. Be assured that this does not imply an overly theoretical approach, but simply one based upon a good engineering foundation. The tutorial will be supported through real-world practical design examples, so one can understand the spirit of the method and the associated design trade-offs in a quantitative and qualitative way. With the breakthrough of a quantitative basis for benchmarking programmable logic architectures, I believe the practice of understanding, selecting, and comparing, PLDs will become a more natural effortless process.

S3
2:30 p.m. - 3:30 p.m.
Design Techniques for FPGAs and CPLDs
Jesse Jenkins, Consultant
PGAs and CPLDs present a paradox. Density benefits are countered with cell limitations and connection restrictions. Successful design techniques conquer these limitations. Count-cell methods, one-hot encoding, flip flop merging and Johnson counters are discussed in depth.

S4
4 p.m. - 5 p.m.
Designing FPGA-Oriented ABEL Code for Efficient State Machine Implementation
Serge Selyutin, Chipcom Corp.
This paper provides hardware designers with a migration path from traditional design techniques, based on PAL-type PLDs, to FPGA-specific design techniques. State machine implementations, based on this approach, result in designs with performance optimized for FPGA architecture.

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S5
9 a.m. - 10 a.m.
The ASIC Design Paradigm
Dev Chakravarty, Digital Equipment
The increasing complexity of ASIC devices through increased functionality, higher gate counts, and increased performance has stimulated the need for design automation. In keeping with these trends, design automation strategies and tools such as logic synthesis, static timing verification, and automatic test pattern generation have matured and become part of the design process. However the growth in ASIC complexity coupled with shrinking product life cycles and increased competitiveness have resulted in increasing pressures to reduce design cycle time and ensure first pass design success. In order to cope with the shrinking design life cycles, an approach is to integrate ASIC Design, Debut and Test into a single process instead of considering them as discrete process entities. The proposal is to develop a framework process that encompasses the Design, Debug and Test process entities, very similar to the CAD Framework strategy that linked Design Entry, Simulation and Layout CAD processes. The session will theorize on the need for this approach followed by a case study that features this integrated approach and the resulting benefits.

S6
10:30 a.m. - 11:30 a.m.
The Economics of Low-Cost ASIC Development
John Frediani & Jim Konsevich, Photonics Corp.
This seminar explores the economics, the risks, and the benefits of establishing a low-cost in-house ASIC development center using PC-based tools from several vendors.

S7
2:30 p.m. - 3:30 p.m.
ASIC Supply Risk Management
Jerry Secrest, Secrest Research
Even the best ASIC suppliers miss delivery schedules. This seminar points out the high risk supply situation and steps that can be taken to assure performance to schedule without pushing out business plans. Product life cycles are so short that there is no time to wait for no risk ASIC supply schedules. This seminar shows the purchaser of ASICs how to recognize high risk conditions and to take steps to improve supply schedule performance by orders of magnitude. This seminar shows how the purchaser of ASICs can affect and monitor the IC supply chain in only a few points to reduce the chance of a supply interrupt to insignificant levels.

S8
4 p.m. - 5 p.m.
ASIC Purchasing Strategies
Joe Borak & Rick Gayle, NCR
This seminar describes the NCR developed toolset which assists in evaluating and managing various aspects of ASIC development and sourcing.

S9
9 a.m. - 10 a.m.
CAD Software: Planning, Evaluating, Negotiating, Purchasing, Proliferating, and Keeping Your Job
Jeff Allison & Sean Murphy, Cisco Systems
This presentation will address many of the common situations that occur in the selection and purchase of commercially available CAD tools. Key topics: Making Methodology Drive Requirements; Make Vs. Buy Decision; Benchmarking; Measuring What You Buy; Common Sales Tactics; Planning for Proliferation with First Purchase; Vendor Management: Hotlines, User Groups & Beta Sites.

S10
10:30 a.m. - 11:30 a.m.
Zen and the Art of Hierarchical Compiling Design in Synopsis
John Cooley, Consultant
Come laugh and throw tomatoes at ESNUG's John Cooley as we discuss various hierarchical

compile strategies within Synopsys. Synopsys neophytes/virgins will be greatly confused.

S11
2:30 p.m. - 3:30 p.m.
A Synthesis-Based Methodology for Top-Down Design of Large ASIC/ASSP Cores
Brad Eltman, HDL Systems
A synthesis-based high level design automation (HLDA) methodology will be presented in two case studies. These studies demonstrate the changes designers must make to effectively use HLDA.

S12
4 p.m. - 5 p.m.
Integrated Top-Down System Modeling: a VHDL-Based Methodology
Paul Clemente, Michael Hajj & Wayne Jessop, Raytheon Corp.
Equipment Division of Raytheon company has developed and implemented a VHD- based top-down design, bottom-up verification methodology. This paper will focus on this top-down design methodology, the heterogeneous EDA tools used to create this seamless environment and highlight a few test cases focusing on this new design paradigm.

Wednesday, September 29, 1993
S13
9 a.m. - 10 a.m.
Test Synthesis: Myth or Reality?
Rob Aitken, Hewlett-Packard
Test synthesis comprises five activities: DFT methodology selection, test circuitry insertion, rule checking, ATPG, and vector translation. No single tool is effective in all areas, but tools can be combined for a workable solution.

S14
10:30 a.m. - 11:30 a.m.
Partial Scan Design Methodologies
Mark Milligan, Sunrise Test Systems
Partial scan promises testable designs without the area and speed constraints often associated with full scan. However, whereas full scan design methodologies have been used for years, partial scan is an emerging technique. This paper presents several design methodologies employing partial scan testing.

S15
2 p.m. - 3 p.m
Extending 1149.1 to a Multidrop System Test Bus
Mark Grabowsky, National Semiconductor
This seminar discusses a practical system test solution that extends the IEEE Std. 1149.1 protocol to a hierarchical/multidrop test bus.

S16
3:30 p.m. - 4:30 p.m.
Validation Methods for First-Time Functional Chip Set
Greg Tollefson, Intel Corp.
The Intel 82430 PCISET chipset for Pentium PCs had functional A-steps. This case study shows the validation methods used to accomplish this.

S17
9 a.m. - 10 a.m.
High-Performance ASIC Design
Chip C. Stearns, Vertex Semiconductor,
High performance ASIC design can no longer be isolated from the total system design. ASIC design techniques/methodologies based upon system constraints are discussed in this seminar.

S18
10:30 a.m. - 11:30 a.m.
Implementing a Low-Power ASIC
Jim Konsevich, Photonics
Battery operation requires reducing the power consumed buy an ASIC by eliminating functions, reducing the speed of operation, and enabling minimum functions at any one time.

S19
2 p.m. - 3 p.m.
A Gate Array in a Day
Mark A. Heuchert, Silicon Graphics
Imagine being able to have a gate array built in a day. Sure PLDs and FPGAs can be programmed in seconds, but sometimes a real gate array is needed. This paper will cover the design cycle of a product, which connected a single workstation-cpu system to four high performance graphic subsystems. A key to the product's development was Chip Express' laser cut gate array technology. The focus will be centered around the product's use and implementation of this technology. Design steps, from high level design considerations and technology selection to product production, will be discussed.

S20
3:30 p.m. - 4:30 p.m.
Design of a High-Speed Interface for 0.5-Micron Gate Arrays
Frank Ramsay, Toshiba America
This seminar looks at high performance I/O buffers for 0.5µm ASICs. These include GTL buffers and PLLs for very tight clock skew control.

S21
9 a.m. - 10 a.m.
Top-Down HDL Modeling
Mike Baird, Sylvan Technology
A modeling methodology for true top-down HDL design beginning with behavioral models. Resultant models may simulate in a system level configuration with mixed levels of models.

S22
10:30 a.m. - 11:30 a.m.
Developing a Self-Optimizing VHDL Model
Mike Lottridge, Consultant
Learn how to modify your VHDL testbench and VHDL models to perform system level optimization using simulated annealing.

S23
2 p.m. - 3 p.m.
Study of an ATM Physical Layer Receiver Design in Verilog HDL
Kien Du Phung & Antonio R. Dimalanta, Jr., National Semiconductor
Our presentation focuses on the top-down design of an Asynchronous Transfer Mode (ATM) Physical Layer Receiver using Verilog HDL and National Semiconductor's Design Automation 4 (DA4) system for ASIC design.

S24
3:30 p.m. - 4:30 p.m.
ASIC Implementation of a Gigabit Per Second Switching Network
Pat Hamilton, Bill Woodruff, TriQuint Semiconductor
TRW implemented two ASICs plus a crosspoint switch to assemble a 512x512 digital switching network. Data rates from 400Mb/s to 1.2Gb/s were implemented. Key issues in systems design, circuit implementation, CAD interface, packaging and test will be highlighted.

Thursday, September 20, 1993
S25
9 a.m. - 10 a.m.
Linear IC Parasitic Element Simulation Methodology
Mark Jakusovszky, National Semiconductor
Attendees will be introduced to a straightforward methodology for parameterizing linear IC parasites, thus greatly simplifying the design process and improving the chances for design success. This methodology will be supported by actual design examples.

S26
10:30 a.m. - 11:30 a.m.
Layout Technique for Minimizing Clock Skew
Hiroyuki Fukuyama, Shuji Nomura & Ichiro Yamamoto, Oki Semiconductor
Describes Oki's automatic layout approach to sub-micron clock distribution that achieves less than 500 ps clock skew without layout limitations or prior dedicated hardware constraints.

S27
2 p.m. - 3 p.m.
Applications of Reconfigurable Logic
Bradly K. Fawcett, Xilinx
Innovative designers are utilizing the "in-system reconfigurability" of SRAM-based FPGAs to construct systems with built-in diagnostics, "adaptable" systems, and systems with "Multi-purpose" hardware.

S28
3:30 p.m. - 4:30 p.m.
Solid-State Client Server Computing in EDA Design
Craig Warner, Ceram Inc.
In order to design next-generation electronics products, designers are forced to use current generation computing resources. Traditional data-storage and network architectures are creating severe bottlenecks in the design process. A new approach, based on advances in low-cost solid-state storage and high speed network-caching, is presented as an alternative to address these bottlenecks.

S29
9 a.m. - 10 a.m.
Fuzzy Logic Cores Provide Powerful Control Solutions
Dennis McCarty, American Neuralogix
The Neuralogix Fuzzy logic ASIC core product line offers the most powerful and inexpensive Fuzzy logic control solution available. The presentation shows the use of Fuzzy logic and the cores in specific applications.

S30
10:30 a.m. - 11:30 a.m.
The Silicon PC Board
David A. Fechser, VLSI Technology Inc.
This seminar deals with the evolution of the custom and semicustom IC business from the early 70s to the 90s. The trends, from full custom projects through gate arrays, standard cells, and megacells, are discussed. This paper discusses the ASIC business of the 90s and how it is growing to resemble the PC board business of the 70s. FSB blocks, cores, and megacells of the future are discussed.

S31
2 p.m. - 3 p.m.
MCM Designs for High-Speed Networks
Doug Bush, National Semiconductor
Designers who need the high speed performance of ECL without the time for new product design cycles have the MCM approach as an option. This seminar discusses the MCM solution.

S32
3:30 p.m. - 4:30 p.m.
Assembled Multichip Module Testing
Dr. London Jin, Vertex Semiconductor
This seminar will provide an overview of assembled multichip module (MCM) testing, and addresses the key issues of what and how to test.

S33
9 a.m. - 10 a.m.
Design Verification: The Reality of Formal Proofs Today
Eugene Y. Zhang, Jackie A. Patterson & Mark D. Noll, Amdahl
This seminar will provide insight into the use of Formal Verification tools to speed ASIC design verification process, and practical experience in evaluation of these tools.

S34
10:30 a.m. - 11:30 a.m.
Is the EDIF Hassle Over?
Rich Goldman, Synopsys Inc.
EDIF V3 0 0 has recently been released. Does this new version resolve the difficulties users had with EDIF V2 0 0, or will it create a new set of problems? This seminar presented by the chairman of the EDIF Technical Committee provides the answer.

S35
2 p.m. - 3 p.m.
Managing the Product Development Process for Revenue and Quality
Gary W. Panzer, Hughes Missile Systems Company
Market share. Sharehold value. Testability. Upgrade capability. Customer support. Integrating business and technical aspects of the product development process will lead companies in reduced time-to-market, lower product costs, improved quality and increased competitive edge.

S36
3:30 p.m. - 4:30 p.m.
A Mixed-Signal Design Metric to Evaluate Design Cycle Time Improvements
Mark R. Rencher, Motorola Inc.
The application of metrics in the EDA area of quantify design cycle time improvements is required. Through research and studies conducted on actual designs a Mixed-Signal Design Metric is presented.

idea'93

September 28-30, 1993
Moscone Convention Center
San Francisco • California

Tuesday, September 28, 1993			
9:00 a.m. 10:00 a.m.	**S1** Notebook Computer Power Management Strategies Employing PLDs *Robert Bielby*	**S5** The ASIC Design Paradigm *Dev Chakravarty*	**S9** CAD Software: Planning, Evaluating, Negotiating, Purchasing, Proliferating, and Keeping Your Job *Jeff Allison* *Sean Murphy*
10:30 a.m. 11:30 a.m.	**S2** Demystifying Programmable Logic with Metric Benchmarks *Jay Sturges*	**S6** The Economics of Lowcost ASIC Development *John Frediani* *Jim Konsevich*	**S10** Hierarchial Compile Strategies *John Cooley*
1:00 p.m. 2:30 p.m.	***Panel Discussion - Life in the Synthesis Jungle***		
2:30 p.m. 3:30 p.m.	**S3** Design Techniques for FPGAs and CPLDs *Jesse Jenkins*	**S7** ASIC Supply Risk Management *Jerry Secrest*	**S11** A Synthesis-Based Methodology for Top-Down Design of Large ASIC/ASSP Cores ***Brad Eltman***
4:00 p.m. 5:00 p.m.	**S4** Designing FPGA-Oriented ABEL Code for Efficient State Machine Implementation *Sergey Selyutin*	**S8** ASIC Purchasing Strategies *Joe Borak* *Rick Gayle*	**S12** Integrated Top-Down System Modeling: A VHDL-Based Methodology *Paul Clemente* *Michael Hajj* *Wayne Jessop*
Wednesday, September 29 1993			
9:00 a.m. 10:00 a.m.	**S13** Test Synthesis: Myth or Reality? *Rob Aitken*	**S17** High-Performance ASIC Design *Chip C. Stearns*	**S21** Top-Down HDL Modeling *Mike Baird*
10:30 a.m. 11:30 a.m.	**S14** Partial Scan Design Methodologies *Mark Milligan*	**S18** Implementing a Low-Power ASIC *Jim Konsevich*	**S22** Developing a Self-Optimizing VHDL Model *Mike Lottridge*
12:00 Noon 1:30 p.m.	***Panel Discussion - Protecting Intellectual Property in the EDA Industry***		
2:00 p.m. 3:00 p.m.	**S15** Extending 1149.1 to a Multidrop System Test Bus *Mark Grabowsky*	**S19** A Gate-Array in a Day *Mark A. Heuchart*	**S23** Study of an ATM Physical Layer Receiver Design in Verilog HDL *Kien Du Phong* *Antonio Dimalanta, Jr.*
3:30 p.m. 4:30 p.m.	**S16** Validation Methods for First-Time Functional Chip Sets *Greg Tollefson*	**S20** Design of a High-Speed Interface for 0.5 Micron Gate-Arrays *Frank R. Ramsay*	**S24** ASIC Implementation of a Gigabit Per Second Switching Network *Pat Hamilton* *Bill Woodruff*
Thursday, September 30, 1993			
9:00 a.m. 10:00 a.m.	**S25** Linear IC Parasitic Element Simulation Methodology *Mark Jakusovszky*	**S29** Designing with Fuzzy ASIC Cores *Dennis McCarty*	**S33** Design Verification: The Reality of Formal Proof Today *Eugene Y. Zhang* *Jackie A. Patterson* *Mark D. Noll*
10:30 a.m. 11:30 a.m.	**S26** Layout Technnique for Minimizing Clock Skew *Hiroyuki Fukuyama* *Shuji Nomura* *Ichiro Yamamoto*	**S30** The Silicon PC Board *David A. Fechser*	**S34** Is the EDIF Hassel Over? *Rich Goldman*
12:00 Noon 1:30 p.m.	***Panel Discussion - Mining the Federal Labs***		
2:00 p.m. 3:00 p.m.	**S27** Applications of Reconfigurable Logic *Bradly K. Fawcett*	**S31** MCM Designs for High-Speed Networks *Doug Bush*	**S35** Managing the Product Development Process for Revenue and Quality ***Gary W. Panzer***
3:30 p.m. 4:30 p.m.	**S28** Solid-State Client Server Computing in EDA Design *Craig Warner*	**S32** Assembled Multichip Module Testing *Dr. London Jin*	**S36** A Mixed-Signal Design Metric to Evaluate Design Cycle Time Improvements *Mark R. Rencher*

Wescon/93

Technical Program

Tuesday, September 28, 1993
9:30AM to 11:30AM
Session 1
MMICS for Wireless Communications
High volume microwave monolithic integrated circuits (MMICs) are required for both the receiver front-ends and the power amplifier modules for cellular and cordless telephones, PCN, WPBX, WLAN, GPS, DBS, and various other wireless communication applications. The pros and cons of silicon and GaAs MMICs for this application will be compared and discussed.
Organizer/Chairman: Dr. Charles Huang, ANADIGICS, Inc.

Tuesday, September 28, 1993
9:30AM to 11:30AM
Session 2
Robotics and Vision Systems
Robots are playing a vital role in the manufacture and assembly of a variety of equipment. Increased sophistication, higher productivity, in addition to superior quality, are some of the benefits of robotic vision. Precise location and detection of faults, particularly in printed circuit boards, has been made possible due to the recent technological developments in vision systems. In this session several experts from a variety of industries discuss design and application aspects of modern instrumentation.
Organizer/Chairman: Dr. Mysore Narayanan, Miami University

Tuesday, September 28, 1993
9:30AM to 11:30AM
Session 3
System-Level Design of Synchronous Memory Based Systems – PANEL
System-level memory design is undergoing a transition from asynchronous to synchronously clocked access to take advantage of newly emerging synchronous DRAM and SRAM devices. This trend, combined with Low Voltage Supply, Low Voltage Swing Interfaces and Solder Ball Grid Array packaging, confront the designer with a staggering array of options, possibilities and risk. This panel will discuss critical issues encountered in the creation of Synchronous Memory Subsystems including Precision Clock Generation and Distribution, Physical Layer Models, Protocol Layer Models and Synchronous DRAM SIMMs.
Organizer/Chairman: Gil Russell, NEC

Tuesday, September 28, 1993
9:30AM to 11:30AM
Session 4
The State-Of-The-Art in Digital Logic Synthesis
In today's highly competitive market, electronic system designers are faced with the conflicting challenges of greater system complexity and the need for short, efficient design cycles. To increase ASIC design productivity, many designers are turning to high-level design languages, such as VHDL and Verilog HDL. Logic synthesis tools are then used to compile the designs to a netlist optimized for the target ASIC architecture. This session will examine the latest synthesis tools, and explore the nuances and trade-offs of using synthesis technology.
Organizer/Chairman: Bradly K. Fawcett, Xilinx Inc.

Tuesday, September 28, 1993
2:00 PM to 4:00 PM
Session 5
Intelligent Communications
Networks in the 90s will need to be more reliable than they are today. This will not be an easy task because as the need for reliability is increasing, the complexity of the network will increase as new services such as multimedia collaborative networking and wireless LAN technology are added to the current networking infrastructure. Communications will need to be more intelligent to meet the new demands of the network's manager and end-users.
Organizer/Chairman: Karen Parker, National Semiconductor

Tuesday, September 28, 1993
2:00 PM to 4:00 PM
Session 6
Image Processing Applications
Engineers and scientists are entering the 21st century on a firm ground of strong technological innovations. Computers, robotics, lasers, vision systems, ASICs, fuzzy logic, neural networks, virtual reality, artificial intelligence, and expert systems are only a few to mention. These have provided engineers and scientists with powerful tools to design sophisticated instrumentation catering to a variety of needs ranging from manufacturing processes to medical diagnostics. In this session several experts from a variety of industries discuss design and application aspects of modern instrumentation, with special reference to image processing techniques.
Organizer/Chairman: Dr. Mysore Narayanan, Miami University

Tuesday, September 28, 1993
2:00 PM to 4:00 PM
Session 7
Applications for Lossless Data Compression
Virtually from nowhere data compression applications have exploded into a $300 million market. Software packages can now double the storage capacity in disc drives while the new V.42 bis standard can double the transmission rate in modems. But the best is yet to come. Applications for image compression and brain-like databases are just around the corner.
Organizer/Chairman: Klaus Holtz, Omni Dimensional Networks

Tuesday, September 28, 1993
2:00 PM to 4:00 PM
Session 8
System Design Techniques for High-Speed Logic
As microprocessors and systems achieve higher speeds and clock rates, "glue logic" has had to improve its performance to keep pace. This session will cover the new considerations brought about by the faster speeds mandated in modern systems. The session will include discussions of new high-speed logic families, system-level simulation of high-speed signals, testability, advanced packaging and the resulting signal integrity.
Organizer/Chairman: Zwie Amitai, A&L Associates - Co-Chairman: David C. Wyland, The Wyland Group

Wednesday, September 29, 1993
9:30AM to 11:30AM
Session 9
Coping with Today's Defense Environment
This session will deal with the issues of surviving in the defense business, defense conversion, downsizing and applying defense technology to the commercial marketplace. Dr. William Perry will lead off with his insights on defense conversion. Other papers will discuss the challenges, in both small and large companies, of conversion to civilian products as well as downsizing and selling off assets. Two papers will discuss survival in the defense arena, one covering use of Total Quality Management and the other discussing defense product offerings that are attractive in a tight budget environment.
Organizer/Chairman: Dr. Bill B. May, ARGOSystems, Inc. (Emeritus)

Wednesday, September 29, 1993
9:30AM to 11:30AM
Session 10
New Developments in Small Rechargeable Batteries for Portable Electronics I
Two sessions are proposed to cover the spectrum of rechargeable battery technology. A brief introduction into the fundamentals of battery technology, definitions and basic thermodynamics will establish the basis for the following discussions. A rationale for the emerging technologies as compared to the mainline systems will be established. A detailed discussion of each of the batteries and their characteristics follows. Next, regulations and pending legislation impacting the use of rechargeable batteries will be reviewed. These regulations impact the user, designer and device manufacturer as well as the battery producer.
Organizer: Ralph J. Brodd, Valence Technology, Inc.

Wednesday, September 29, 1993
9:30AM to 11:30AM
Session 11
Antifuse-Based Field Programmable Gate Arrays
Field Programmable Gate Arrays (FPGAs) combine the logic integration benefits of custom VLSI circuits with the design, production, and time-to-market benefits of a user-programmable device. Advances in FPGA technology are expanding the range of viable applications for these versatile devices. This session will examine the latest advances in the architecture of antifuse-based FPGA devices.
Organizer: Bradly K. Fawcett, Xilinx Corp. - Chairman: Dennis McCarty, Actel Corp.

Wednesday, September 29, 1993
9:30AM to 11:30AM
Session 12
Opportunities in Intelligent Transportation – I
The Intelligent Vehicle Highway Systems (IVHS) are applying electronic technology to improve safety and efficiency, and to reduce congestion and pollution on the nation's highways. Major demonstration projects and operational deployments are underway or being planned throughout the country which will encourage and rely on many new commercial products and services. Part 1 of this two-part session will provide an overview of the national and California IVHS programs with special emphasis on the present and planned Southern California programs in Los Angeles, Orange and San Diego counties.
Organizer/Chairman: Dr. Lawrence E. Sweeney, Jr., Etak, Inc.

Wednesday, September 29, 1993
12:30 PM to 2:30 PM
Session 13
Career Transition from Defense to Commercial (Panel)
A panel discussion by engineers who have made the conversion from defense to commercial will discuss the challenges, pitfalls, and successes of making the transition and their advice to others on steps to take. Each member will briefly discuss his career and their experiences in making the conversion. About an hour will be reserved for questions from the audience.
Organizer: Dr. Bill B. May, ARGOSystems, Inc. (Emeritus) - Chairman: David Markus, Markus Executive Search

Wednesday, September 29, 1993
12:30 PM
2:30 PM
Session 14
New Developments in Small Rechargeable Batteries for Portable Electronics II
Organizer: Ralph J. Brodd, Valence Technology, Inc. - Chairman: David M. Butze, Valence Technology, Inc.

Wednesday, September 29, 1993
12:30 PM to 2:30 PM
Session 15
SRAM-Based Field Programmable Gate Arrays
By combining the density and flexibility of a gate array with the convenience, ease-of-use, and time-to-market benefits of a user-programmable device, Field Programmable Gate Arrays (FPGAs) have become the fastest growing segment of the IC market. Advances in FPGA technology are expanding the range of viable applications for these versatile devices. This session will examine the latest advances in the architecture of static-memory-based FPGA devices.
Organizer/Chairman: Bradly K. Fawcett, Xilinx Corp.

Wednesday, September 29, 1993
12:30 PM to 2:30 PM
Session 16
Opportunities in Intelligent Transportation – II
This is the second part of a two-part session on commercial opportunities in Intelligent Vehicle Highway Systems (IVHS) programs. Part 2 will describe on-going and planned IVHS programs in Northern California including a planned Bay Area traveler information system and a traffic management system already in operation in San Jose. A variety of research efforts underway in the UC PATH program will be described including work in automatic vehicle control systems. Finally, representative opportunities in IVHS consumer products will also be presented.
Organizer/Chairman: Dr. Lawrence E. Sweeney, Etak, Inc.

Wednesday, September 29, 1993
3:00 PM to 5:00 PM
Session 17
Technical Advances in Defense Electronics
This session comprises five papers on direction finding and signal processing in the collection of radar and radio signals in defense applications. Traditional problems in the intercept of signals involve determining the direction (and perhaps location) of these signals in an environment with numerous interfering signals and the classification or identification of these signals.
Organizer: Dr. Bill B. May, ARGOSystems, Inc. (Emeritus) - Chairman: William Bigas, Condor Systems, Inc.

Wednesday, September 29, 1993
3:00 PM to 5:00 PM
Session 18
Energy Management for Portable Power Sources
Designers are challenged to find new ways to optimize power sources in portable devices. At the design stage, factors like drop out voltage, line voltage and quiescent current need to be considered in order to maximize product performance in portable devices like cellular phones, portable laptops and recorders. This session will examine the recent developments in solid state, resistors, capacitors and other analog devices.
Organizer: Charles F. Byers, Hayes/Gardiner - Co-Organizer: Charles M. Smaltz, Micrel Semiconductor - Chairman: Larry Sample, Micrel Semiconductor

Wednesday, September 29, 1993
3:00 PM to 5:00 PM
Session 19
Complex Programmable Logic Devices
Extending and expanding the familiar and/or planned architecture of simple PLDs, Complex Programmable Logic Devices (CPLDs) can implement thousands of gates of logic at high, predictable performance levels. This session will examine the architectures of the latest generations of CPLD devices.
Organizer: Bradly K. Fawcett, Xilinx Corp. - Chairman: Jeffrey Goldberg, Xilinx Inc.

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Wednesday, September 29, 1993
3:00 PM to 5:00 PM
Session 20
Safety and Its Impact on the Vehicles of the Future – PANEL
The demand for an automotive safety feature is growing in importance as auto makers design in more systems offering driver and passenger air bag, antilock brake and traction control, and collision avoidance systems.
Organizer/Chairman: Diane Norman, Electronic Buyers' News (EBN)

Thursday, September 30, 1993
9:30AM to 11:30AM
Session 21
Developments in Fuzzy Logic and Neural Netwoks – I
Fuzzy logic has emerged as one of the most significant developments in how we perform, control, think, and compute. This session will present various developments in the field of fuzzy logic, including an overview of fuzzy, fuzzy and neural-nets, simulation of fuzzy, and tuning a fuzzy system.
Organizer: Yoke Tanaka, Togai InfraLogic - Chairman: Camerone Welch, Togai InfraLogic

Thursday, September 30, 1993
9:30AM to 11:30AM
Session 22
Prototype Circuit Board Fabrication
Regardless of whether an OEM follows traditional or concurrent engineering product development paths, sooner or later a prototype of the design must be built. And, of the three major stages in the creation of a prototype - namely design, assembly, and test – this session will focus on the assembly of prototype printed circuit boards and modules, as this stage is undergoing considerable technological change.
Organizer/Chairman: Joseph J. Spadaro, EE Product News Magazine

Thursday, September 30, 1993
9:30AM to 11:30AM
Session 23
New Developments in HDTV Wafer and Integration Technologies
High definition TV is now under intensive investigation in the U.S. The first half of this session provides a sample of the technologies involved in order to make HDTV a commercial reality. The topics are: HDTV Standards Converter and High-Speed Adaptive Equalization. The second half of the session deals with the on-going improvements in fabricating the integrated circuits on the semiconductor for all the sophisticated applications. The development of dedicated IC's and new electronics applications must be going hand-in-hand.
Organizer/Chairman: Bill Wun, Hewlett-Packard Company - Co-Chairman: George H. Allen, Apple Computer

Thursday, September 30, 1993
9:30AM to 11:30AM
Session 24
Electric Vehicle Technology
The future of the electric car depends heavily on battery technology. This session will explore several developments in battery technology, including an advancement in the thin film polymer battery, and improvements in the conventional lead acid battery. The session will also cover fast charging of electric vehicle batteries, as well as precision energy monitoring to measure battery energy.
Organizer: Zdenek (Stan) E. Skokan, Electric Vehicles Inc.

Thursday, September 30, 1993
12:30 PM to 2:30 PM
Session 25
Developments in Fuzzy Logic and Neural Networks – II
Fuzzy logic is not just for toasters anymore. This session looks at the diverse areas to which fuzzy logic is being applied from control to medicine to finance to information processing.
Organizer: Yoke Tanaka, Togai InfraLogic - Chairman: Camerone Welch, Togai InfraLogic

Thursday, September 30, 1993
12:30 PM to 2:30 PM
Session 26
Specialty Memory Advances Improve System Performance
To keep pace with higher performance requirements, IC designers and users must turn to architectural advances and innovations. Merging logic into the memory ICs provides higher system performance. Examples of such innovations are the use of different memory cells and user-friendly interfaces. This session will describe new product features, applications examples of specialty memories, and will touch on the trends and direction of this technology.
Organizer/Chairman: Zwie Amitai, A&L Associates - Co-Chairman: Mark Muegge, Quality Semiconductor, Inc.

Thursday, September 30, 1993
12:30 PM to 2:30 PM
Session 27
Digital Video
Much has been discussed about image compression, a key technology for digital video, but other elements of the system have been ignored. This session examines some of the other needs in a digital video system that directly affect image quality.
Organizer/Chairman: Richard Quinnell, Cahners Publishing Company

Thursday, September 30, 1993
12:30 PM to 2:30 PM
Session 28
Using the PC Architecture in Embedded Applications
There has been growing interest in using the IBM PC (and PC/AT) for non-desktop, "embedded" applications. Benefits of doing this include reduced development costs, accelerated time-to-market, and improved product features. Advantages, disadvantages, and enhancements to the PC architecture are discussed, and alternative implementations are compared. The session will consist of five 20-minute presentations (see below), followed by a brief panel discussion featuring all the speakers answering questions from the audience.
Organizer/Chairman: Rick Lehrbaum, Ampro Computers, Inc.

Use the scheduling grid on page 22 to schedule your Wescon days.
For registration information, see page 35. To register for *idea'93*, use the form on page 23.

Wescon/93

September 28-30, 1993
Moscone Convention Center
San Francisco, California

ROOM	120	121	123	124
Tuesday, September 28, 1993				
9:30 a.m. to 11:30 a.m.	*Session 1*	*Session 2*	*Session 3*	*Session 4*
	MMICS for Wireless Communications ***C. Huang***	Robotics and Vision Systems ***M. Narayanan***	System-Level Design of Synchronous Memory Based Systems (PANEL) ***G. Russell***	The State-Of-The-Art in Digital Logic Synthesis ***B. Fawcett***
2:00 p.m. to 4:00 p.m.	*Session 5*	*Session 6*	*Session 7*	*Session 8*
	Intelligent Communications ***K. Parker***	Image Processing Applications ***M. Narayanan***	Applications for Lossless Data Compression ***K. Holtz***	System Design Techniques for High-Speed Logic ***Z. Amitai***
Wednesday, September 29, 1993				
9:30 a.m. to 11:30 a.m.	*Session 9*	*Session 10*	*Session 11*	*Session 12*
	Coping with Today's Defense Environment ***B. May***	New Develop. in Small Rechargeable Batteries for Portable Electronics -- I ***R. Brodd***	Antifuse-Based Field Programmable Gate Arrays ***B. Fawcett***	Opportunities in Intelligent Transportation -- I ***L. Sweeney***
12:30 p.m. to 2:30 p.m.	*Session 13*	*Session 14*	*Session 15*	*Session 16*
	Career Transition from Defense to Commercial (PANEL) ***B. May***	New Develop. in Small Rechargeable Batteries for Portable Electronics -- II ***R. Brodd***	SRAM-Based Field Programmable Gate Arrays ***B. Fawcett***	Opportunities in Intelligent Transportation -- II ***L. Sweeney***
3:00 p.m. to 5:00 p.m.	*Session 17*	*Session 18*	*Session 19*	*Session 20*
	Technical Advances in Defense Electronics ***B. May***	Energy Management for Portable Power Sources ***C. Byers***	Complex Programmable Logic Devices ***B. Fawcett***	Safety and Its Impact on the Vehicles of the Future (PANEL) ***D. Norman***
Thursday, September 30, 1993				
9:30 a.m. to 11:30 a.m.	*Session 21*	*Session 22*	*Session 23*	*Session 24*
	Developments in Fuzzy Logic and Neural Networks -- I ***Y. Tanaka***	Prototype Curcuit Board Fabrication ***J. Spadaro***	New Developments in HDTV Wafer and Integration Technologies ***B. Wun***	Electric Vehicle Technology ***S Skokan***
12:30 p.m. to 2:30 p.m.	*Session 25*	*Session 26*	*Session 27*	*Session 28*
	Developments in Fuzzy Logic and Neural Networks -- II ***Y. Tanaka***	Specialty Memory Advances Improve System Performance ***Z. Amitai***	Digital Video ***R. Quinnell***	Using the PC Architecture in Embedded Applications ***R. Lehrbaum***

Program subject to change.

For final dates, times and places, consult the Wescon Official Program or call (800) 877-2668, ext. 250.

INFORMATION MUST BE FILLED OUT COMPLETELY IN ORDER TO PROCESS COMPLIMENTARY REGISTRATION

Principal job function (CHECK ONLY ONE)

A ❑ General & Corp. Mgmt.
B ❑ Design & Development Engineering
C ❑ Purchasing & Procurement
D ❑ Manufacturing & production
E ❑ Software Development
F ❑ Engineering services (test, QC, staff)
G ❑ Marketing
H ❑ Sales
I ❑ Ad, media, public relations
J ❑ Professor, student, library
K ❑ Other (please specify)_____

Primary End Product (CHECK ONLY ONE)

L ❑ Personal computers
M ❑ Workstations
N ❑ Other computers (mini, mainframe, super)
O ❑ Computer peripherals
P ❑ Communication systems
Q ❑ Avionics, marine, space, electronics
R ❑ Military
S ❑ Industrial controls, systems, equipment robotics
T ❑ Software manufacturer/developer
U ❑ Office & business machines
V ❑ Computer systems integrator
W ❑ Automotive/other ground vehicles
X ❑ Medical electronic equipment
Y ❑ Electronic instrumentation/ATE/design & test equipment
Z ❑ Consumer electronics, appliances
AA ❑ ICs & semiconductors
AB ❑ Other components, materials, hardware & supplies
AC ❑ Electronic subassemblies (boards, modules, power supplies)
AD ❑ Other_____

My principal responsibility (CHECK ONLY ONE)

CE ❑ Management other than engineering
CF ❑ Engineering Management
CG ❑ Engineering
CH ❑ Other (please specify)_____

Design Responsibilities (CHECK ALL THAT APPLY)

CA ❑ Chip
CB ❑ Board
CC ❑ Systems
CD ❑ Other (please specify
CE ❑ None of the above

Please check all that you recommend, specify or use:

ASICs
AE ❑ PLDs
AF ❑ FPGAs
AG ❑ Gate arrays
AH ❑ Cell-based
AI ❑ Full custom
AJ ❑ Analog/mixed-signal
AK ❑ GaAs
AL ❑ BiCMOS
AM ❑ ECL
AN ❑ Multichip modules
AO ❑ Standard product semiconductors (processors, chipsets, ASSP)
AP ❑ VLSI packaging
AQ ❑ Design services
AR ❑ Contract manufacturing
AS ❑ Embedded ASICs

Electronic design automation tools, hardware
AT ❑ Workstations
AU ❑ Personal computers
BA ❑ Verification/emulation tools
BB ❑ Programmers
BC ❑ IC design & analysis
BD ❑ PCB design & analysis
BE ❑ Test & instrumentation equipment
BF ❑ Networking equipment
BG ❑ File servers
BH ❑ Development tools and systems
BI ❑ Hardware accelerators
BJ ❑ Computer peripherals

Electronic design automation tools, software
BK ❑ Software for IC design & analysis
BL ❑ Programmable logic design software
BM ❑ PC-based design software
BN ❑ Design entry tools
BO ❑ HDL tools
BP ❑ SPICE software
BQ ❑ IC layout tools
BR ❑ Frameworks
BS ❑ Signal analysis
BT ❑ Fault simulators
BU ❑ Design for test tools
BV ❑ Behavioral models
BW ❑ Software for PCB design & analysis
BX ❑ VHDL tools
BY ❑ None of the above

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No refunds will be made after September 23, 1993.

For more information, call: (800) 877-2668 ext. 244 or (310) 215-3976.

Wescon/idea Product Showcase

These companies are exhibiting exciting new products at this year's show. Please stop by their booth and tell them you saw it in the *IEEE Grid!*

Xenotronix Introduces High Performance, Cost Effective Lead-Acid Battery Charger
Wescon Booth #1256

Xenotronix Inc., Valencia, California, is now manufacturing the HPX-10 series of battery chargers for lead-acid batteries. The HPX-10 series charges batteries to a maximum of 10 watts. All of the chargers in the HPX-10 series are dual stage and fully automatic.

The HPX-10 series feature full metal chassis, reverse and short circuit protection, temperature compensation, and fold back current limiting to ensure charger protection on shorted batteries. Now available from stock, the HPX-10 chargers are priced at $21.96 each in quantity 1000.

For more information, call 1-800-624-XENO.

Tanner Research
idea Section, Booth #2438

Powerful ASIC design software from Tanner Research bring performance and affordability to PCs, Macintoshes, and UNIX workstations.

Tanner Tools TM consist of a complete schematic entry, simulation, layout and verification package for ASIC design.

Tools include the S-Edit TM schematic editor, L-Edit TM layout editor, L-Edit/DRC design rule checker, L-Edit/Extract general device extractor, L-Edit/SPR standard cell place-and-route module, and LVS netlists comparison module.

For digital requirements, GateSim TM provides gate-level timing simulation, and T-Spice TM offers circuit simulation for analog and digital designs.

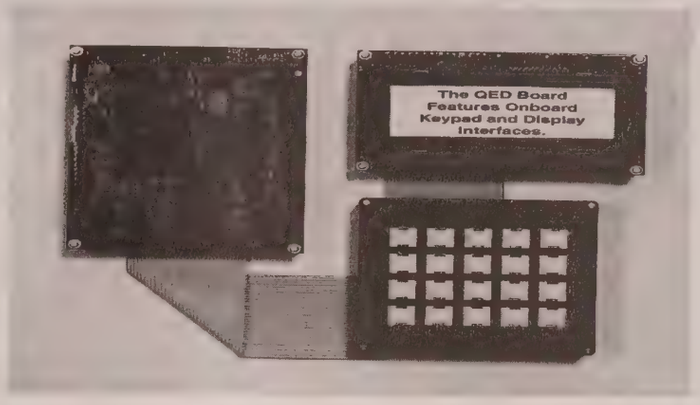
Tanner Research, 180 North Vinedo Avenue, Pasadena, CA 91107
Stop by the booth and ask for your free gift.

FUJITSU MICROELECTRONICS, INC., ELECTRONIC COMPONENTS DIVISION
WESCON BOOTH #6456

A stacked memory card connector will be a featured product at Fujitsu Microelectronics, Inc., Electronic Components Division's Wescon booth this year. The FCN565 series accepts Types I, II and III memory cards and meets all JEIDA and PCMCIA specifications.

The connector consists of two vertically stacked, 68-position, right-angle headers, and is available in various board-mounted heights. Contact pitch is 0.050" x 0.050" for each card slot. Ejection mechanisms are also available in a variety of configurations.

Call 1-800-642-7616 for product information.



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FUJITSU MICROELECTRONICS, INC., ELECTRONIC COMPONENTS DIVISION WESCON BOOTH #6456

Featured at Fujitsu Microelectronics, Electronics Components Division's Wescon booth is the FKB1406, a standard palmtop-type keyboard. The FKB1406 measures 216 mm x 76 mm x 9.7 mm, and provides 84- to 101-key functionality in applications that include sub-notebook, palmtop and pen PCs; office automation and test equipment; and portable instrumentation.

The keyboard features 15 mm key spacing, a 1.5 mm keystroke, and weighs 80 grams. English, UK, French, German, Italian and Swedish versions are available. Semi-custom configurations, including customer-specific colors and legends can also be produced.

Call 1-800-642-7616 to request product literature.

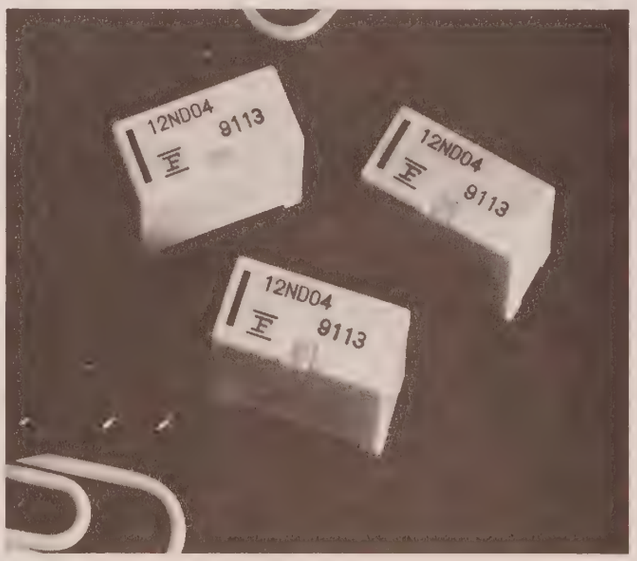
Ultra-Miniature 10mm Thick Fans From Evox Rifa, Inc. Wescon Booth #6409

EVOX-RIFA has introduced a new line of 10mm thick sub-miniature fans from Shicoh Engineering of Japan. These ultra-thin fans are ideal for spot cooling of microprocessors, instrumentation, medical equipment, computer components, and other equipment.

The series is available in four sizes: 25mm square, 40mm square, 52mm square and 60mm square; all 10mm thick. Precision brushless construction provides more than 50,000 hours life and extremely low noise. $7 to $9 in quantity 1000.

For more information, call 708-948-9511

FUJITSU MICROELECTRONICS, INC., ELECTRONIC COMPONENTS DIVISION WESCON BOOTH #6456



Fujitsu Microelectronics, Inc., Electronic Components Division is highlighting its low-power telecom relay at Wescon. The FBR12 relay meets the Bellcore 2,500-volt surge isolation specification required of the next-generation telecom systems.

Its small size and low, 14 mW power consumption also makes the FBR12 suitable for use in test equipment, medical electronics, and temperature control systems.

The FBR12 features a 250VAC switching voltage (max.), 2.0A switching current (max.), and 60W, 62.5VA (max.), 1.0A resistive.

Call 1-800-642-7616 to request product literature.

WESCON SHORT COURSES

Moscone Convention Center
San Francisco, California

	Tuesday, September 28, 1993		
9:30 a.m. to 12:30 p.m.	***SC1*** Fine Pitch Surface Mount Technology ***P. Marcoux***	***SC2*** Applications of Neural Networks and Fuzzy Logic ***D. Wyland*** ***Z. Amitai***	
2:00 p.m. to 5:00 p.m.	***SC3*** The ISO 9000 Quality Standard ***B. Wun*** ***J. Turino*** ***W. Robertson***	***SC4*** PC-Based Multimedia ***C. Wagner***	
	Wednesday, September 29, 1993		
9:30 a.m. to 12:30 p.m.	***SC5*** High-Speed Board Design ***Z. Amitai*** ***D. Wyland***	***SC6*** U.S. Government Services for International Trade ***R. Shea*** ***B. Pata***	
2:00 p.m. to 5:00 p.m.	***SC7*** Introduction to Fuzzy Logic ***Y. Tanaka***	***SC8*** Doing Business in Canada **R. Cohen** **P. Jones** **R. Armstrong**	***SC9*** Accelerated Product Development ***O. Kopelman***
	Thursday, September 30, 1993		
9:30 a.m. to 12:30 p.m.	***SC10*** Design for Testability ***R. Hanson***	***SC11*** Cache Design Demystified ***J. Handy***	***SC12*** Competitive New Product Development ***D. Anderson***
2:00 p.m. to 5:00 p.m.	***SC13*** The Boundary-Scan Std JTAG/IEEE 1149.1 ***R. Hanson***	***SC14*** System Design Using the Pentium™ Processor ***Intel***	

Pre-registration is encouraged. Registration at the door will be accepted on a first-come, first-serve basis with no guarantee of space or class materials. **No refunds will be made after Thursday, September 23, 1993.**

Fee for registration is $20. A special registration discount of $10 is available for IEEE members who register prior to September 3, 1993.

For more information call 800-877-2668 ext. 244

BAY AREA ENGINEER

San Francisco Bay Area IEEE *Calendar Section* *August 1993*

A Brief Walk Through The IEEE-Part I

by Tom Kirsch, past Council Chairman

Based on "An Introduction to the IEEE" A slide presentation prepared by the Directors of the IEEE

The IEEE logo displays vectors for electricity and magnetism - what we call the "right hand rule." During discussions in 1962 that led to the formation of the Institute, one of our members roughed out what has become the IEEE logo. The design uses the diamond from one of our predecessor organization's pins, representing Benjamin Franklin's famous kite.

The Institute incorporates two previous organizations: the American Institute of Electrical Engineers (AIEE) and the Institute of Radio Engineers (IRE). The AIEE was formed on May 13, 1884. Coincidentally, the IRE was formed on the same date in 1912. We officially became the IEEE in 1963. Over the years, distinguished members have included such luminaries as Edison, Bell and Marconi.

The Institute leads in the field of electrotechnology - encompassing everything from aerospace and electronic systems to vehicular technology. The IEEE is an individual membership society - no organizations, no companies. The Institute has three objectives:

Scientific/Educational - to advance the theory and practice of electrotechnology.

Professional - to advance the standing of members of our profession.

Societal - to improve the quality of life through application of electrotechnology and promote public understanding of electrotechnology.

Stop now if you are getting sleepy or bored! Get a cup of coffee, find a comfortable chair, then, please read on to find out more about each of our Institute's objectives.

Scientific/Educational Objectives

First, the Institute is a learned society in that its primary objective are scientific and educational - advancing the theory and practice of electrotechnology. We have coined the word "electrotechnology" to sum up what we're concerned with; namely, electrical, electronics and computer engineering, computer science and the related arts and sciences.

The IEEE serves the profession through its publications, meetings and education programs. We support precollege education, university accreditation and continuing education programs. With the most prestigious technical awards program in the world, the Institute provides recognition for excellence.

Professional Objectives

The IEEE establishes goals for advancing the standing of members in the engineering profession, and provide information to the public on engineering and technology. Through the United States Activities (formerly the United States Activities Board, or USAB), the IEEE supports the professional careers and technology policy interests of U.S. Engineers.

The Institute surveys and reports on matters of concern to members, works with other groups for the benefit of the profession, and recommends standards for qualification and ethical conduct.

Societal Objectives

The IEEE strives to enhance public recognition of the profession, further interests of the Institute and its members in the public arena, and foster a better understanding of the impact of electrotechnology on society. IEEE Public Relations undertakes programs that promote the public understanding and societal contributions of electrotechnology.

IEEE Membership

The IEEE is the world's largest technical professional organization in the world. We are almost three times as large as the second such group, the American Association for the Advancement of Science. And we are global instead of being exclusively U.S. oriented.

Membership has grown steadily since 1963, increasing roughly three per cent annually until 1978. Between 1978 and 1991 our ranks were increasing at four percent a year. The high unemployment years, 1991 to 1992, growth was flat.

Continued on page 34

The Seven Sins (and Remedies) of Quality Rapid Product Development

by Orion Kopelman

Much has been written about how to reduce time to market to compete in the global technology race of the '90's. Why do some companies consistently do it, and others just keep trying? Does one management methodology work better than another?

The majority of Silicon Valley's new product development projects run on schedules that now span less than one year. Estimates tell us that collective human scientific and technological knowledge doubles every year and a half, and may double annually by the year 2000.1 Clearly, we must integrate new information quickly, and get it out to the market in the form of a quality product that generates profit. We must learn to succeed while changes occur at an accelerating pace around us.

Most technology management at least acknowledges this challenging environment. Some companies have adjusted and even thrived on it. However, bad habits have kept the majority of companies stuck in the past. The most common malignant practices in the industry are the seven sins of Quality Rapid Product Development2:

1. Trying to do too much in one project.
2. The NIH—Not Invented Here—syndrome.
3. Not everybody buys-in to a common product vision.
4. Functional organizations refuse to relinquish control to project teams.
5. A weak project team leader, or one that lacks authority.
6. A poor product development process, or none at all.
7. No "Chicken Test" on a working prototype early in the schedule.

The first two, trying to do too much and NIH often go hand in hand. By not using technology available from previous projects or on the outside, you create a monster size endeavor. These "megatrap" projects will rarely complete on schedule. For example, in the mid-1980's a California company spent five years and $15 million to develop a printed circuit board that fit into a slot in a personal computer, and provided 10 MB of hard disk storage to the then floppy-only systems. They developed their own electronics board, thin hard disk that fit in one slot in PC's, and the firmware. A competitor decided to buy a commercially available 20 MB hard disk that took up one and a half slots and mated it to an off-the-shelf controller card. By just writing some firmware, they managed to spend three months, $100,000, and ship a product with double the capacity for the same price, ahead of the other company! More recently, NASA and McDonnell actually developed a prototype of a reusable rocket, the Delta Clipper,. on schedule and within budget (18 months, $60 million. By comparison a recent re-design of the space shuttle toilet cost the taxpayers $23 million...). They achieved this by using "hand-me-downs" ¾ a guidance system from an F-15 jet fighter and some leftover fuel tanks from another program.

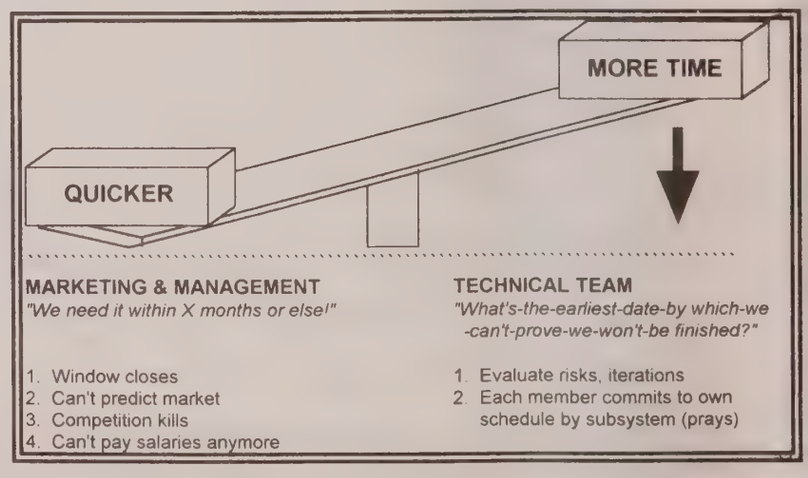
So the solution to avoiding these two sins lies in recognizing that particularly in the '90's, we must become incremental innovators, rather than inventors. Innovation can be defined as: introducing novelty (new know-how) into practical use (technology) to increase the customer's value and satisfaction obtained from the seller's or manufacturer's resources. Lots of technology already exists, untapped, and more and more gets invented at a shocking pace. The US. issues over 300 patents per day! Over 200 million scientists and technologists go to work everyday, more than the number of people that lived on the whole planet 2000 years ago. Why not package available inventions as a subsystem in your product? There's plenty of profit margin for all, if you find the right application.

Furthermore, you must become adept at playing the game of completing as many development cycles as possible, each one resulting with a salable, desirable product. This incremental approach means swinging for base hits. Sometimes these singles can turn into doubles or triples, or even homeruns. By introducing successive generations regularly, a practice perfected by many Japanese companies, you can lower overall risk while learning more about the market and the technology and continuously refining your products. Best of all, you rarely strike out completely and always get paid by the customers along the way. They win, too, since you presumably provide them with value and a better way to do something.

Even the engineers, marketeers, and other project team members win in the long run. But management must steer them clear of their natural tendencies to want to invent everything by themselves, and to have it ready for the product that must ship next month. Technical people usually underestimate the number of unknowns that arise during the development process. So categorize each innovation as minor, medium, or major risk, and carefully justify its benefits and return on investment. By combining minimal invention, taking advantage of existing technology, and introducing a limited number of innovations, everyone comes out ahead on an ongoing basis.

3. Not everybody buys-in to a common product vision.

To successfully innovate incrementally, the company must agree on a clearly defined, limited set of product objectives. Too often not everyone buys into the emerging vision of the product. This results in either technical failures or delays. For example, in one company where marketing and engineering were at odds with one another, a specification called for a quick two week redesign of a door on an armored vehicle to make it "airtight". Unfortunately, the spec. also stated a maximum rate of air leakage allowed. Engineering decided to meet the numerical specification, and of course the customer had expected "airtight" to mean zero leakage. Eventually a team had to be sent to the country that purchased the vehicles to retrofit a totally new design. A simple "slam-dunk" project turned into an eleven week fiasco.


MORE TIME
QUICKER
MARKETING & MANAGEMENT
"We need it within X months or else!"
1. Window closes
2. Can't predict market
3. Competition kills
4. Can't pay salaries anymore
TECHNICAL TEAM
"What's-the-earliest-date-by which-we -can't-prove-we-won't-be finished?"
1. Evaluate risks, iterations
2. Each member commits to own schedule by subsystem (prays)

The obvious, but seldom followed remedy involves getting the whole project team to get together and hash out a written one-page vision. The chart below shows the careful balancing act that "See-Saw Scheduling and Specifications" (SSSS) requires. Everyone must participate in a negotiation process of trading off product features, benefits, and costs for the resulting amount of time and budget required for design and production. The goal is to have all team members commit whole-heartedly and knowingly to a set of milestones that delivers a product to the customers and makes financial sense for everyone. Total buy-in assures Doing It Right the First Time (DIRFT) rather than the second or third.

4. Functional organizations refuse to relinquish control to project teams, and

5. A weak project team leader, or one that lacks authority.

Management experts have touted the concept of organizing companies along the lines of project teams since the beginning of the Space Age. In 1959 Paul O. Gaddis warned in one of the first articles on "The Project Manager" that, "The United States today faces the enormous problem of how to regain undisputed technological leadership.... Advancement ... will shape our future and determine our survival or extinction.... The role of project management will be challenging, exciting, and crucial." This rings as true today as then. And yet many functional managers refuse to give up control over their domain of influence. Managers must recognize that their workers' loyalty must lie first and foremost with small interdisciplinary project teams, chartered with rapidly developing a product. Association with a department like sales or quality becomes secondary.

In part as a result of the layers of entrenched functional middle managers, the wrong project leaders get selected, or don't really have the authority to accomplish their mission. For example, a company making a linear accelerator for cancer therapy with digital control and a computer interface, chose by default the Engineering Manager as the team leader. His lack of experience in linear accelerator technology caused the end product to not meet spec., take four years instead of three, and come in 50% over budget. Similarly, a company making lasers to correct far-sightedness had three people periodically assume the role of project leader. None agreed on an overall approach or schedule. Worse yet, no one person had the responsibility of identifying the major hurdle on the project: insufficient software resources. The project was shipped in 12 months instead of nine, ironically two months after a competitor introduced a comparable product!

Top management must take the initiative to choose the right team leader, and give them all the authority they need to meet their huge responsibility, including forcing a matrix, project-oriented organization chart. "Of all the decisions management makes in managing accelerated new product development, none is more crucial to success than the choice of a team leader. A strong leader will be able to overcome many other shortcomings and imperfect management decisions, but a mediocre one will be stymied even by small obstacles."3 So find an obsessed leader that is confident (yet honest), technical, a model worker, a people person, and has high standards and management ability. Then formally announce their vital role to everyone that must help them.

6. A poor product development process, or none at all.

The Carnegie Mellon Software Engineering Institute has observed five maturity levels in the software development process (see table). These can apply to any process, including new product development. Most Silicon Valley manufacturing organizations operate between levels four and five, whereas project development efforts utilize levels one to three. Only a very few highly successful companies have graduated to the higher levels. Most of these will also have a guidebook to serve as a cookbook for predictably following a recipe every time to develop quality new products quickly.

Recently, a company developed a balloon catheter designed for coronary angioplasty, with a potential gross yearly sales of $100 million over a two year window. Despite use of a corporate plane, the project stalled while transferring it from California's engineering group to the manufacturing plant in Mexico. Production people only voiced concerns after equipment had arrived, not early in the project. The lack of a well defined process resulted in a three month delay that cost the company about $5.6 million in lost profit. The clear lesson is to make product development a process that's worked on continuously and as importantly as on any project.

7. No "Chicken Test" on a working prototype early in the schedule.

Every project undergoes a critical test which serves as a reality check. It finally tells us if the essential technology actually functions as it should. This is called the Chicken Test4. It gets its name from tests performed on airplane jet engines. Namely, in order to ascertain that during flight the engines can contend with the ingestion of flocks of birds, a barrel gun several feet in diameter fires live chickens at them. This serves as an early warning system to uncover a possible fundamental flaw in the design, before spending the whole $250 million necessary to develop a new engine. Every project must eventually persevere a chicken test before it can really take off. The only question is how late in the project you discover that you may need to take a different approach. Obviously, the earlier the better.

For example, a major mainframe computer manufacturer decided to re-package its systems into a new market application, telecommunications switching. Nine months into the one year project they attempted system integration for the first time. Unfortunately, like many companies that hope for everything to just work out perfectly, many of the mechanical subsystems didn't fit together. Over 180 drawings had to be redone, causing a three month delay in a highly contested market. To avoid this kind of late breaking bad news, you must simply have the courage to spend a little extra time and money early on in the project. Do your "Chicken Test" on a working prototype (even without having all the bells and whistles yet) within the first 25% of the schedule. This way you can find out if you're really on track, or need to alter your course. With a typical one year schedule, you could fail the test at the 90 day mark, start over, and still probably ship a product ahead of your competition who had to do massive rework later in their project.

Summary:

Sluggish product development can cost companies thousands of dollars in lost profit per day, due to late entry into the market. Consider the fact that 60% of Hewlett Packard's revenue comes from new products introduced in the last two years. To survive and thrive in a leapfrog world where even current products are here today and obsolete tomorrow, you must learn to develop new products swiftly. If you found your sins on this list, confess them and choose to change, transform, and become a Quality Rapid Product Development company of the 90's and the next millennia. Many companies like yours already practice acceleration techniques and routinely develop products in half the time that it used to take!

Please see footnotes on page 34

Orion Kopelman serves as President of Global Brain™, Inc., a company synergizing technology and consciousness. He has taught Rapid Product Development at UC Berkeley Extension since 1991 and has helped many Silicon Valley companies develop products more rapidly. Previously, he was Chairman of IEEE's Santa Clara Valley Engineering Management Society, and Vice President of Mountain Computer, Inc. during a six year growth spurt from 50 to 500 people. On October 4-5 he will present an IEEE-sponsored course titled "Blitzkrieg Rapid Product Development" in Santa Clara, CA. Please contact Global Brain, Inc. at 415/327-2012 (by phone or fax) for registration information.

Council Activities and Actions

Reported by Tom Kirsch

At our May meeting the SFBA Council the following resolution was passed unanimously:

"Resolution of the San Francisco Bay Area Council of The IEEE

Be it resolved that all nominees for Chapter or Section Officer will be screened by the Sections to be sure all nominees meet qualifications to hold office in accordance with IEEE Bylaws.

Be it resolved further that if Field Services, Section/Chapter Services, Piscataway, NJ, determines that an officer is ineligible to hold office, they shall notify the Section Chairperson, by phone (preferably), or, by writing, of the ineligibility and request appropriate resolution. The ineligible officer is not to be contacted directly regarding his/her qualifications."

The issue surrounding this resolution pertains to the manner in which Field Service handled the case of Ms. Susan MacKensie, the Chairperson of the newly-formed Computer Society Chapter in the San Francisco Section, who was not qualified to hold the office of Chairperson.

There are many ways of dealing with the problem of officer ineligibility and it is concluded that any problems can be better dealt with at the local level. The Section Directors who are members of the SFBA Council are committed to the spirit and content of the resolution and have initiated a review process at the Section level.

The Council Has Purchased a New Display System

At its May meeting, the Council authorized $7,500 for the purchase a display system and graphics to enhance our image at job fairs and other IEEE activities.

The IEEE sponsors the Westech and Lendman job fairs and is given booth space at both. The Westech booth space is 10 ft. and the Lendman space is in a vestibule area adjacent to an elevator; size in excess of 10 ft.

The Council will purchase a 10 ft display system from Skyline Displays in Sunnyvale. This is the same company that supplied the Wescon display system. The display will be purchased with continuous shelving and continuous periodical racks, four curved 30 " panels, and lights. Over the next six months graphics for the display will be added that will become either a permanent part of the display or a removable Velcro picture. The theme at fairs will be about jobs for job fairs and how the IEEE can help. Future graphics will be developed for or by both our Sections and Chapters so that they may use the display at their own conferences and meetings.

INET'93 - Towards a Global Community International Networking Conference

The International Networking Conference is the annual conference of the Internet Society, a new professional society serving the Internet community. INET'93 will be held on 17-20 August 1993 at the Hyatt Embarcadero in San Francisco. Focusing on worldwide issues of research and academic networking, the goal of INET'93 is to bring together individuals from university, industry and government who are involved with planning, developing, implementing, managing and funding national, regional and international research, academic, and commercial networks.

The conference agenda will include plans and status reports on research and academic networks throughout the world. The Program consists of six parallel tracks:

Network Technology: Advances in the Network Technology Base

Network Engineering: Building the Global Infrastructure

Application Technology: Enabling Technologies for Distributed Applications

User Applications: Support for International Communities of Interest

Regional Issues: Networking Around the Globe

Policy Issues: Governance, Management, and Financing of International Networks

The conference will be held immediately preceding INTEROP 93 Fall, the leading conference and exhibition for Internet technologies.

The Advance Program is available via anonymous ftp from mordor.stanford.edu as

~ftp/pub/inet93/Advance.Program.PS/ (directory of PostScript files),

~ftp/pub/inet93/Advance.Program.txt (text version)~ftp/pub/inet93/INET93.Advance.Program.PS.tar.Z (compressed tar directory)

For further information, send an email message to request@inet93.stanford.edu or contact Elizabet Barnhart barnhart@educom.edu

202-331-5342

CALL FOR PAPERS

1994 International Reliability Physics Symposium

The 1994 International Reliability Physics Symposium will be held April 11-14 at the Fairmont Hotel in San Jose. Building in reliability continues to be the cornerstone of the symposium's program. Papers are being solicited that illustrate the incorporation of reliability physics, reliability engineering, design for maximum performance margin, fabrication, assembly, and manufacturing process control to improve system reliability.

The identification of new microelectronic failure mechanisms, improved insights into existing failure mechanisms, and new or innovative analytical techniques continue to be the mainstay of the 1994 event. Papers dealing with reliability of advanced packaging techniques for multichip modules are also requested.

The following topics are considered to be of prime interest:

–Building in reliability for Si, GaAs, and optoelectronic devices.

–Testing methodologies for reliability.

–Analyzing for reliability.

Prospective authors should submit a one-page, 50-word abstract, and a two-page summary. Deadline to receive this material is October 1, 1993. Mail to:

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Photo Highlights of the SCV Section Banquet

Sid Hollander, SCV member of the IEEE Public Affairs Committee, chronicled the June 17 Section banquet. Here are a few of the highlights.

Guests mingled at the reception prior to adjourning to the dining room

SCV Science Fair winners, Gina Marrello and Melinda Marks

Outgoing Council Chairman Tom Kirsch addresses the audience

SCV PACE Chair, Carolyn Koenig was there to award the Science Fair winners

Outgoing SCV Section Chairman, Harry Gill was Master of Ceremonies

Featured speaker for the event was noted author, George Gilder

Incoming SCV Section Chair, Jim Lamb accepts the gavel from Harry Gill

Incoming Council Chairman, Art Astrin receives congratulations from Tom Kirsch

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BS in electrical engineering (92) Cal Poly. Studied power quality, protection, Fortran, C and Unix. Have EIT State of Calif. Member IEEE PES. Have many years experience in industrial plant construction and maintenance as an electrician. Want entry level position either with an engineering firm or a large plant located on the Central Coast from San Jose to King City.

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Contact Subash Krishnankutty at 415-285-4931

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Contact Chet Shirali at 415-897-7483

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Contact Marc J. Deshaies. 415-493-7415

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over 14 years in data communications with 6 years management experience. Built and managed a quality engineering test group to validate a range of communications products including X.25 packet switches, SNA, Bisync, Async PADs, Ethernet LAN routing bridge, SUN Unix based network management system, T1 Multiplexer, UTS (mainframe Unix) based front end processor products

John Humphreys at 510-792-5441

email: jhump@infoserv

JUNIOR ELECTRICAL ENGINEER

VLSI circuit and logic design, IC layout, circuit and logic simulation. Have MSEE (Dec '92) degree from San Jose State University. Dependable, self-motivated and industrious. Willing to be trained and to work hard and quickly acquire necessary skills. References available on request.

Contact Mukesh Patel at 408-773-1229

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Skilled engineer with strong aptitude for digital and microprocessor based design. Recently completed projects include a microprogrammed controller utilizing ISP HDL, a volatile memory design using Viewlogic design tools, and a real-time data acquisition system including a DMA controller. Eleven years of technical experience with eight years of troubleshooting and repair of Unix based machines including SPARC with Sun Microsystems. Ability to program in C and Pascal. Recent BSEE at SJSU.

Contact Harley Halseth at 408-262-2545

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System architect and general problem solver with more than twenty years experience in conceptual, system and architectural design of major communications and computer systems. Possess a track record demonstrating highly innovative designs manifesting outstanding manufacturability and maintainability. Have extensive analog and digital circuit design background and software assistance. Seeking association with some brighter individuals who have questions.

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Footnotes from page 29

1 Russell, Peter. 1992. The White Hole in Time, Our Future Evolution and the Meaning of Now; Harper SanFrancisco, p. 28. A dazzling and innovative picture of humanity, that integrates evolutionary perspective and a startling vision of what the future means to the living in today's eternal present.

2 Kopelman, Orion. 1993. Guidebook for Quality Rapid Product Development. Global Brain™, Inc., Palo Alto, CA, USA, 1993. A very practical handbook of checklists and bullet-style guidelines that can be followed in a cookbook-like manner. Presents a management methodology that when followed rigorously, results in significantly improved time to market and return on R&D investment!

3 Reinertsen, Donald and Smith. 1991. Developing Products in Half the Time. Van Nostrand Reinhold. An excellent book, a precursor of Quality Rapid Product Development.

4 Peters, Tom and Austin, Nancy. 1985. A Passion for Excellence, The Leadership Difference. Random House, p. 130. Very insightful information on innovation and particularly "Skunkworks."

Wescon Short Course

from page 4

He will be joined by a panel of three experienced value engineering consultants from different fields who will be available to answer questions at the end of the course.

The cost for this course is $20 and includes class handouts. IEEE members who register by September 3 will pay just $10 for this course. For more information and to register, call JoAnn Lindberg at 1-800-877-2668-X244.

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A WAlk Through The IEEE

from page 27

The membership in 1993 is close to 320,000 members in 150 countries. Currently we have 37 technical societies worldwide. The three largest societies are Computer, Communications and Power Engineering. Members can choose from a diverse range of technologies and applications. Societies were first introduced in 1948, following World War II, beginning with the Audio Group - now the Signal Processing Society.

In addition to technical specialties, societies cover education, engineering management, professional communications and social implications of technology - reflecting the broad scope of the IEEE. Technical societies' memberships range from 2,000 to 100,000; average membership is 10,000. More than 60 percent of our members belong to one or more technical societies.

Total society memberships exceeded Institute memberships for the first time in 1978, showing the importance members attach to their technical specialties. In 1992, there were 908 chapters of our 37 world-wide societies.

IEEE Regions

The Institute is divided into 10 regions. The first six are in the United States. The remaining four are Region 7 - Canada, Region 8 - Europe, the Middle East and Africa Region, 9 - Central and South America, including Puerto Rico, and Region 10 - Southeast Asia and Australia.

The main IEEE local unit is a Section. We have 284 Sections worldwide; 174 in the United States. The Santa Clara Valley Section is the largest Section in the world with over 13,000 members. Tokyo is the largest Section outside the United States and could soon surpass the Santa Clara Valley Section. Some 26% of IEEE members live outside the United States.

As you might imagine, the largest concentration of U.S. membership is along the Northeast corridor from Boston to Washington and on the West Coast. Regions 1 through 6 have approximately 108,000 members combined, reflecting the high concentration of engineers in the eastern and western United States.

To be continued -

Please note that the membership data contains an error. Have you caught it? The September issue will contain the correction.

Next Month in the Grid . . .

The new season opens in September with new programs, seminars and short courses. The center pages of the September issue of the *Grid* will contain your 1993-1994 roster of officers. We suggest you remove the pages and keep the directory for future reference. This year we are listing e-mail addresses of all Section and Society chapter officers who have connected to the IEEE e-mail network through Infoserv. If you haven't joined this network, all you need is a PC, Mac or Unix machine equipped with a modem. Call the Council Office for more information.

This issue of the *Grid*, as well as last month's, carried details on Wescon and *idea'93*. Our September issue will bring you any updated news that's available.

INFORMATION MUST BE FILLED OUT COMPLETELY IN ORDER TO PROCESS COMPLIMENTARY REGISTRATION

Title (CHECK ONLY ONE)
Management:
JA ❑ President, Owner, Chairman
JB ❑ Vice President
JC ❑ Director
JD ❑ Department Head
JE ❑ Section Head
JF ❑ Project Engineer
JG ❑ Senior Engineer
JH ❑ Other Management

Engineering/Other Staff
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JM ❑ Mfg. Engineer/Production
JN ❑ MTS
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MG ❑ Test, measurement, ATE, Instruments
MH ❑ Data Acquisition Products
MI ❑ PCs
MJ ❑ Engineering Workstations/Hardware
MK ❑ EDA Software Tools
MT ❑ Engineering Software
ML ❑ Local Area Networks
MM ❑ Computer Peripherals
MN ❑ Subsystems/Board Level Products
MO ❑ Power Supplies, including Batteries
MP ❑ Production Equipment/Machinery
MQ ❑ Production Supplies/Materials
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KF ❑ Software Development
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KJ ❑ Student
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LB ❑ Automotive/Other Ground Vehicles
LC ❑ Avionics, Marine, Space Electronics
LD ❑ Communication Systems
LE ❑ Components, Materials, Hardware Supplies
LF ❑ Computer Peripherals
LG ❑ Computer Systems Integrator
LH ❑ Computers
LI ❑ Consumer Electronics
LJ ❑ Contract Engineering, Manufacturing
LK ❑ Distributor
LL ❑ Education
LM ❑ Electronic Instrumentation, ATE, Design & Test Equipment
LN ❑ Electronic Subassemblies
LO ❑ Industrial Controls, Systems
LP ❑ Medical Electronic Equipment
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